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A STUDY OF COMMUNICATION PROCESSOR SYSTEMS

Wayne State University

Tse-yun Feng
Dharma P. Agrawal

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A communication processor system (CPS) is expected to fulfill the requirements of both communication and computing functions. Hence, major characteristics pertaining to these two aspects are reviewed and their relative merits are carefully examined.

At present, there are hundreds of CPS's now in operation or in planning. Among them, several of the important systems considered and the major emphasis

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is given to those systems which have recently been proposed by various organizations to the government agencies. Such a restriction is justified by the fact that a new evolved architecture is expected to overcome most of the shortcomings and limitations of the existing systems. General descriptions of the systems included here are those proposed by: North Electric Company, GTE Sylvania, Carnegie-Mellon University, Honeywell, and RCA Corporation.

An attempt is made to obtain a comparative statement of various parameters and the uniqueness of these systems so that their salient features and deficiencies can be compared. Finally, our recommendations and architectural strategies are outlined to provide guidelines for CPS design. Further thorough investigation is necessary in order to obtain more precise architectural requirements of CPS's.

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EVALUATION

Many Communication Processors (CP) were not designed specifically for communication processing but were selected from commerically available processors and adapted to this application. Performance deficiencies relating to these processors are therefore to be expected. These deficiencies along with future communication demands require careful evaluation in light of today's dramatically changing technology so that cost-effective Communication Processor Architecture designs may be effected.

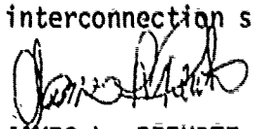
The recent advances in LSI technology has caused significant changes in the field of computer architecture. One trend is to construct a processing system by interconnecting a large number of processors and memory modules. Key to this approach is the design of an efficient intercommunication network which can avoid the bottlenecks introduced by the traditional bi systems and enhance its system performance in terms of availability, reliability, and throughput. Also involved is the processing unit design. The processing unit should include features for enhancing processing power within chips, improving testability and system reliability.

Similar considerations can be used to design the CPS. However, the performance of a CPS is only partially dependent on the computation effectiveness, thus architectural decisions have to be taken to fulfill the communication requirements.

This report discusses the communication and the architectural considerations that characterize the salient features of a CPS. In addition, it provides the relative advantages of different approaches currently prevalent in existing or proposed systems.

This effort's significance is both to architectural trends which take advantage of low cost commercially available microprocessor technology and to the application of this technology to the field of communications. As such, it has relevance to TPO's R3A and R3D.

This report will be disseminated to the communications community. Follow-on efforts will focus strictly on the multistage interconnection strategy for architectures in general.



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Project Engineer

CHAPTER I

GENERAL CONSIDERATIONS

1. Introduction

A communication processor system (CPS) can be defined [1] as a collective entity of all operations and logic processes which, when properly configured, would be capable of performing a wide range of communication applications including circuit switching, store-and-forward switching, or a combination of these two functions. In store-and-forward switching either the message switching is implemented or the packet switching technique is utilized.

While most circuit switching CPS's are specifically designed, the overwhelming majority of other CPS's are not originally designed for communication applications. In most cases, they are commercially available systems adapted for this purpose. In these CPS's, the presence of some performance deficiencies is quite natural. Even in the processors specifically designed for circuit-switching functions, there exist some limitations. Future communication demands in commercial, government, or military applications induce intensive investigations to be carried out so that proper evaluation of these deficiencies and limitations may lead to a new computer architecture that will better fit in the projected requirements.

The recent advances in LSI technology has also caused significant changes in the field of computer architecture. One trend is to construct a processing system by interconnecting a large number of processors and memory modules. The key questions for this approach is to design an efficient intercommunication network which can avoid the bottlenecks introduced by the traditional bus systems and enhance its system performance in terms of availability, reliability, and throughput. Another question involves the processing unit design. The newly designed processing unit should include features for enhancing processing power within chips, improving testability and system reliability.

Similar considerations can be used to design the CPS. However, a dominant factor influencing the performance of a CPS is the

effectiveness of the communication handling techniques. The design objective of the computing system is only partially dependent on the computation effectiveness and the architectural decisions have to be taken to fulfill the communication requirements [2]. This leads to an approach which differs from the conventional design criterion.

In the following, we discuss the communication and the architectural considerations that characterize the salient features of a CPS. In addition, we provide the relative advantages of different approaches currently prevalent in the existing or in the proposed systems.

2. Communication Considerations

Several factors such as the communication technique, the communication network characteristics, the network structure, and the network design need to be examined when designing a communication system. Those factors are briefly discussed below.

A. Communication Technique

The communication techniques are critically important as there could be more than one decision point along a path set up in an intercommunication network. There are at least two communication levels: source-to-destination and switching-point-to-switching-point. There are three possible switching methodologies for supporting general networking requirements:

1. circuit switching,
2. packet switching, and
3. integrated circuit-packet switching.

The circuit switching involves the establishment of a dedidated path between any two terminals and the connection is disrupted only when ony one of the two users signals for such action. This switching technique is relatively inefficient for transmission of short messages. But, it is more suitable for transfer of bulk data.

In contrast to circuit switching, packet switching attempts to multiplex the use of the communication circuit among all related terminal units. Messages are typically broken into a series of fixed length, addressed packets of data which are

routed independently to their destination using store-and-forward procedures. The packet switching can partially solve the blocking problem of interconnection networks. However, it also increases the complexity of the control procedure and the effective time delay.

The integration of circuit and packet switching into a unified switching concept [3] enables efficient and economical use of the communication system. It also allows a better connection between the terminals. This Slotted Envelope NETwork (SENET) concept utilizes constant period, self-synchronizing master frame to convey messages to the multi-node network. The assignment of compartments to different types of traffic provides both circuit switching and packet switching capabilities simultaneously. The characteristics of different subscribers have been used to separate three different classes of traffic [3]. These classes and associated parameters are given in Table 1.1. The size of the compartments for each group of traffic is allowed to vary dynamically with the instantaneous traffic conditions and is achieved by performing the frame composition and decomposition at each node. Each envelope begins with a header and the end is recognized by a trailer.

B. Communication Network Characteristics

The characteristics which can be used to specify the intercommunication network are identified as follows:

1. topology of interconnection network,
2. control structure of interconnection network,
3. logical complexity,
4. blocking probability,
5. message response time,
6. system capacity or throughput,
7. network reliability,
8. sensitivity,
9. traffic bottleneck or deadlock,
10. transmission error rate, and
11. cost.

TABLE 1.1

Subscriber Classes and Associated Parameters

Class of Subscriber	Characteristics	Initial Connection Time	Virtual Connection	Error Control	Cross-Network Delay	Service
I	Long messages requiring continuous real-time delivery (voice, facsimile, video)	Several seconds	Connection is to be maintained for several minutes	Not required	Small fraction of a second	Call may be blocked if network is busy
II	Short discrete messages requiring near real-time delivery (inter-active data)	Several seconds	Each subsequent interactive exchange short (500 bits) may be extended over a number of hours	Required	Average of less than one second	Call is always accepted provided destination subscriber is available
III	Long messages requiring neither continuity nor immediate delivery (bulk data)	Several seconds	Connection is required for several minutes	May or may not be required	Could be several minutes	Call is always accepted but prerogative of system to temporarily delay or restrict service

C. Network Structure

The cost and performance of the intercommunication network depends greatly on the network structure as the designer chooses. The network structure in the form of cross-bar switches is a widely utilized circuit-switching technique for establishing a connection between any two users. The maximum number of simultaneous connections set-up between various subscribers can be achieved only if each cross-point is capable of providing conflict-free parallel switching. Since the number of cross-points grows exponentially with the number of subscribers, the cost of the circuitry required for the switching facilities becomes significantly high when the number of subscribers is large. The solution to this problem at the cost of set-up time is the use of multi-stage network structures where the network is partitioned into several stages and the desired connection is established via intermediate stages. The cost advantage offered by the multi-stage network is partially off-set by the control selection time. However, multistage network usually provide multiple path connections and are, therefore, more fault-tolerant than cross-bar switches. The current trend is to utilize the multistage network as effectively as possible.

There are four types of multistage interconnection networks [4]:

1. strictly nonblocking network,
2. wide-sense nonblocking network,
3. rearrangeable nonblocking network, and
4. blocking network.

A strictly nonblocking network allows connection between any two lines regardless of the current connections. A wide-sense nonblocking network provides the same service if specific routing rules are observed. The rearrangeable nonblocking network also has the same capability except that it requires alterations in the existing connections. The blocking network can perform many but not all possible connections.

Generally speaking, the nonblocking property is not the prime criterion for choosing network structure. Network structure with

properties of easy manufacturing, low cost, simple control, graceful degradation, and short delay time are the major parameters.

D. Network Design

The hardware design considerations for the interconnection network are:

1. cross-bar switches versus multistage design,
2. central versus distributed control,
3. linkage versus connection capability,
4. circuit partitioning and chip types,
5. number of interconnection points versus system reliability, and
6. synchronization.

The network software design is essentially to have a set of basic control procedures to ensure an efficient, correct and smooth transfer of information in the interconnection network system. The basic control procedure can be partitioned into the following four categories [5,6]:

1. communication protocols,
2. flow control procedures,
3. graceful degradation considerations, and
4. routing procedures.

3. Architectural Considerations

The evolution of the CPS architecture shows that the trend has been from uniprocessor architecture to multiple-processor architecture either in circuit switching [7-12] or in store-and-forward switching [13-14] and the interconnection technique tends to be full connection [15]. Current proposals [12,16-21] of CPS architectures also show that a CPS with the capability of performing integrated circuit and store-and-forward switching (e.g. SENET) is preferred. Thus, various attributes of interconnection organizations such as the transfer strategy, the control method, the path structure, and the system topology are used to classify the actual system designs [1].

Based on the interconnections between various functional units of a computer, the present day multiple-processor systems can be

classified into the following categories:

A. Time-Shared or Common Bus Systems

In this organization, the complexity depends on the number of buses and their functional usage. The simplest single bus system allows communication between various constituent units via the common bus and at any time only one path can exist between a sending and a receiving unit. The use of multiple buses allows more parallelism. The only drawback of such systems is the requirement of additional bus control signals. An example of such systems with multiple buses is the one proposed by GTE Sylvania Inc. [18].

B. Cross-Bar Switching Systems

The cross-bar switches provide nonblocking simultaneous memory accesses and communications among other functional units. With this interconnection organization, the maximum number of transfers that can take place simultaneously is limited by the number of memory units and the bandwidth-speed product of the buses rather than by the number of paths available.

The system can be expanded by adding additional modules of crosspoints. But the number of crosspoints grows exponentially with the number of switching ports. Carnegie-Mellon C.mmp is a good example of such a system.

C. Multiport Memory Systems

In this organization, the control, switching and priority arbitration logic is concentrated at the interface to the memory units. Each processor has access through its dedicated bus to all memory units. Memory access conflicts are resolved by assigning permanently designated priorities to each memory port.

Possible access to all memory modules by each processor through its associated bus leads to a very high transfer rate. But, the multiport memory system requires a large number of processor-memory interconnections. An example of such a system is the IBM 360/67.

D. System with Multistage Interconnection Networks

Many of the large computer systems that are being used and designed today have interconnection networks either between processors and memory modules or between subsystems with each system consisting of a processor-memory pair. In most of these systems, the interconnection networks constitute the heart of the system.

Depending on functional requirements, the control scheme and other factors, there exist several variations of interconnection networks. The multistage network allows the desired communications in a more general way than the other three organizations. One of the examples of such a system is the flip network in STARAN [24].

E. Other Systems

Some systems have mixed interconnection organization. The Pluribus system [13] having memory and I/O buses is an example. This system is used as a modular switching node for the ARPA network. It consists of seven dual processors sharing two banks of multiport structured memory modules.

Basically these characterizations are derived from the existing systems. However recent advances in LSI technology have caused a significant change in the field of computer architecture. It is quite obvious that any further significant increase in processing speed can be obtained only by concurrent processing of several data sets and the feasibility of incorporating as many as 10^5 functional modules in a single complex computer system is no more questionable. Of course, the hardware cost is not of major concern any more.

Some of the problems like synchronous switching, central control, graceful degradation, routing techniques, and full connection can be easily tackled by cost effective LSI implementation of the interconnection organization. In turn, this requires minimization of the number of module types and not the number of components utilized. Functionally and physically partitioned modules not only make them suitable for LSI implementation, but

allow the use of the same software control program developed for a single module. Projection from the past progress in LSI technology, we may foresee that the most complex computer system of today can be fabricated on a small number of chips in the near future [27].

4. Report Organization

The major characteristics pertaining to the communication and computing aspects of the CPS have already been reviewed. The relative merits of communication aspect have been covered in Chapter II [31,32]. Chapter III analyzes the performance, reliability, and life cycle cost of various multi-processor architectures [29]. Among hundreds of CPS's now in operations or in planning, this report includes only those systems which have recently been proposed. Such a selection can be justified by the fact that whenever a new architecture is to be evolved, attemps are made to overcome all the shortcomings and limitations of the antecedent systems. Moreover, newer systems are expected to reflect the current state-of-the-art.

Chapter IV through VIII covers the general description and evaluation of several proposed CPS's. A brief concluding remark indicating the potential adoption of the system is also included towards the end of each chapter. Some of the existing communication systems are briefly described in Chapter IX. Finally, the comparison of the proposed systems and our own recommendations are outlined in Chapter X.

CHAPTER II
NETWORK ANALYSIS CORP. STUDY OF INTEGRATED DOD VOICE AND DATA NETWORKS

1. Introduction

The report prepared by Data Network Corporation [31,32] presents a comparative study of three potential network design strategies of circuit switching, packet switching and hybrid switching for DOD voice and data communications requirements. Recent advances in computer and communications technologies further make this study important. Three basic aspects covered in this report are:

1. the economics of serving voice and data applications on a common integrated communications system,
2. the comparison of alternative switching technologies for integrated voice and data networks, and
3. the cost-effectiveness of alternative voice digitation rates and strategies.

The digital conversion of analog voice waveform and transmission in digital form offers advantages such as a greater immunity to interference and compatability and ability to serve voice and data traffic with a common integrated system. In addition to voice and data communication, future Department of Defense (DOD) requirements can be given by the following:

1. conferencing,
2. multidestinations message dispatching,
3. computer generated voice response,
4. automatic speaker authentication, and
5. computer recognition of speech content.

The future data traffic is assumed to be 36.15 Mbps with a composition of 50% bulk and 50% interactive data. System costs are also obtained for data throughputs of 11.6 Mbps, 86.8 Mbps and 202.4 Mbps. The effect of 675 Erlangs and 1350 Erlangs of voice load on the cost and performance is also considered. The digitation rate of the voice available in analog form is expected in the range

of 2.4 kbps to 64 kbps. This makes the ratio of voice and data traffic to vary from 3:97 to 94:6 percent.

2. Description of Switching Strategies

The transmission of future voice and data traffic is possible using the following switching strategies:

A. circuit switching,

B. hybrid switching (circuit/packet), and

C. packet switching.

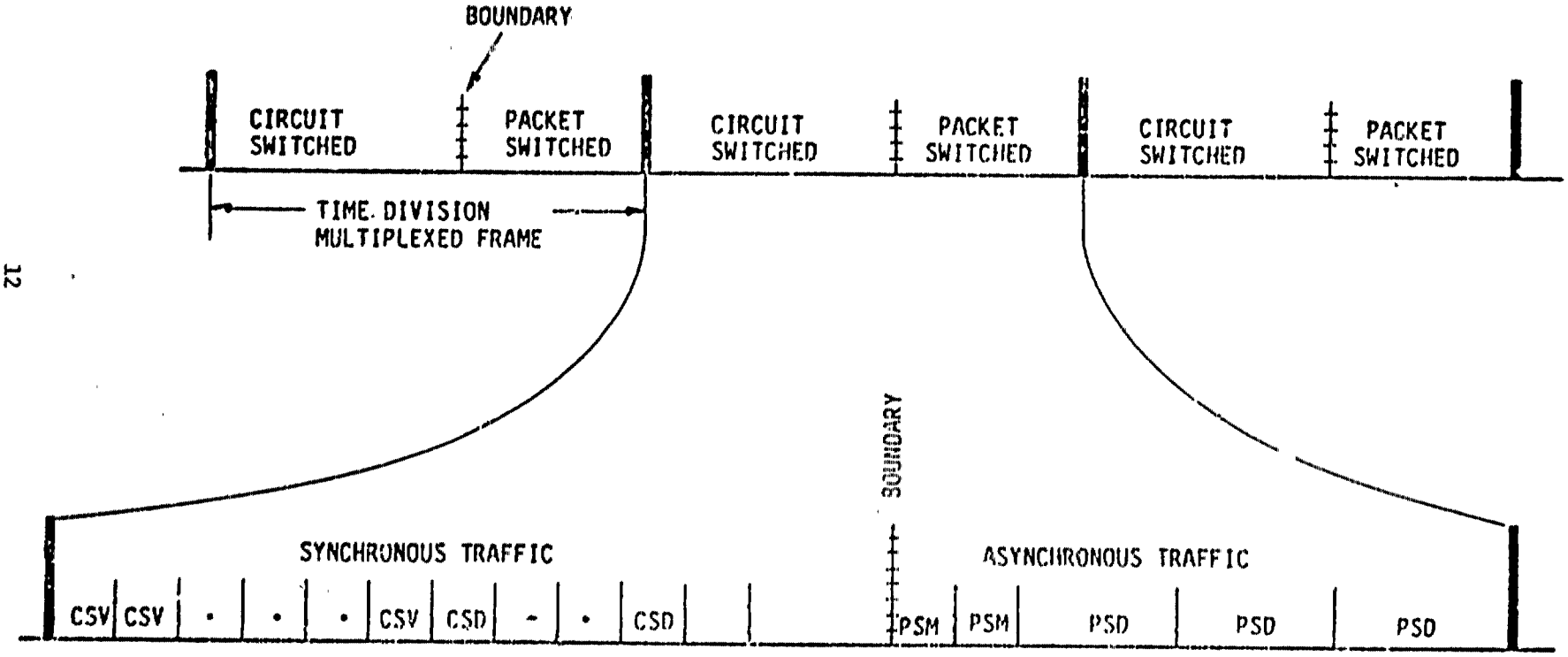
In the following, these techniques are briefly discussed.

A. Circuit Switching

In circuit switching, the associated transmission facilities are reserved once an end-to-end circuit has been established between the calling and the called subscribers. The circuit setup is achieved either by "origination office control" or on a link-by-link basis by "progressive routing". This type of conventional circuit switching is utilized for voice and bulk data applications. But, for interactive data users, the circuit setup continues only during the message transmission. This is known as fast circuit switching. In ideal circuit switching, the setup time is assumed to be zero.

B. Hybrid Switching

Hybrid switching tecunique allows integration of voice and data applications by dynamically sharing the switching and transmission facilities between traffic using the circuit switching (for voice) and packet switching (for data) modes. The hybrid system employs a constant period master frame which consists of several slots for the two types of traffic. The structure of such a frame is shown in Fig. 2.1. The voice and data are multiplexed on the circuit switched region while signalling messages for circuit setup/disconnection and interactive data are included in the packet switched region. The packet header includes all necessary information to ensure a unique reassembly into the original message.



CSV - Circuit Switched Voice Slot
CSD - Circuit Switched Data Slot
PSM - Packet Switched Signaling Message Slot
PSD - Packet Switched Data Slot

Fig. 2.1 Examplary hybrid switching channel structure: Time division multiplexed frame

Two hybrid switching options are investigated. The first is the fixed boundary frame management where the frame partition between circuit-switched and packet-switched traffic is fixed. The second type is moveable boundary frame. This does have an assigned boundary but the unutilized part of circuit-switched mode can be dynamically assigned to the packet-switched traffic.

C. Packet Switching

In voice communication, an end-to-end full duplex channel is utilized only for a fraction of time. Packet switching eliminates the wastage of transmission capacity during the silence periods in the voice conversation. This concept is utilized in a network shown in Fig. 2.2. In this network structure, a periodic analysis of speech indicates the active state of the speaker and the digitized form of only the part that is transmitted, as the silent part contains no information and nothing is transmitted from the hand-set. Thus, packetizing of digitized voice and data is done at the source switch and store-and-forward procedures are utilized. At the destination, the digital representation is used to create a synthetic version of the original speech.

The transmission of digitized voice can be done using either a fixed path protocol or a path independent protocol. In the fixed-path protocol, the originator signals messages to setup a path while no path is set up in the path independent protocol and each packet is transported to the destination independent of other packets of the same conversation.

Thus, any one of these three techniques can be utilized for information transmission. But the performance of a network greatly depends on the network structure. Another important aspect is the cost-effectiveness of including voice digitation devices of varying rates. Three different alternatives of placing the digitation process are:

1. the backbone network voice requirements are in digital form at a given bit rate,
2. voice is digitized at the origination backbone node, and

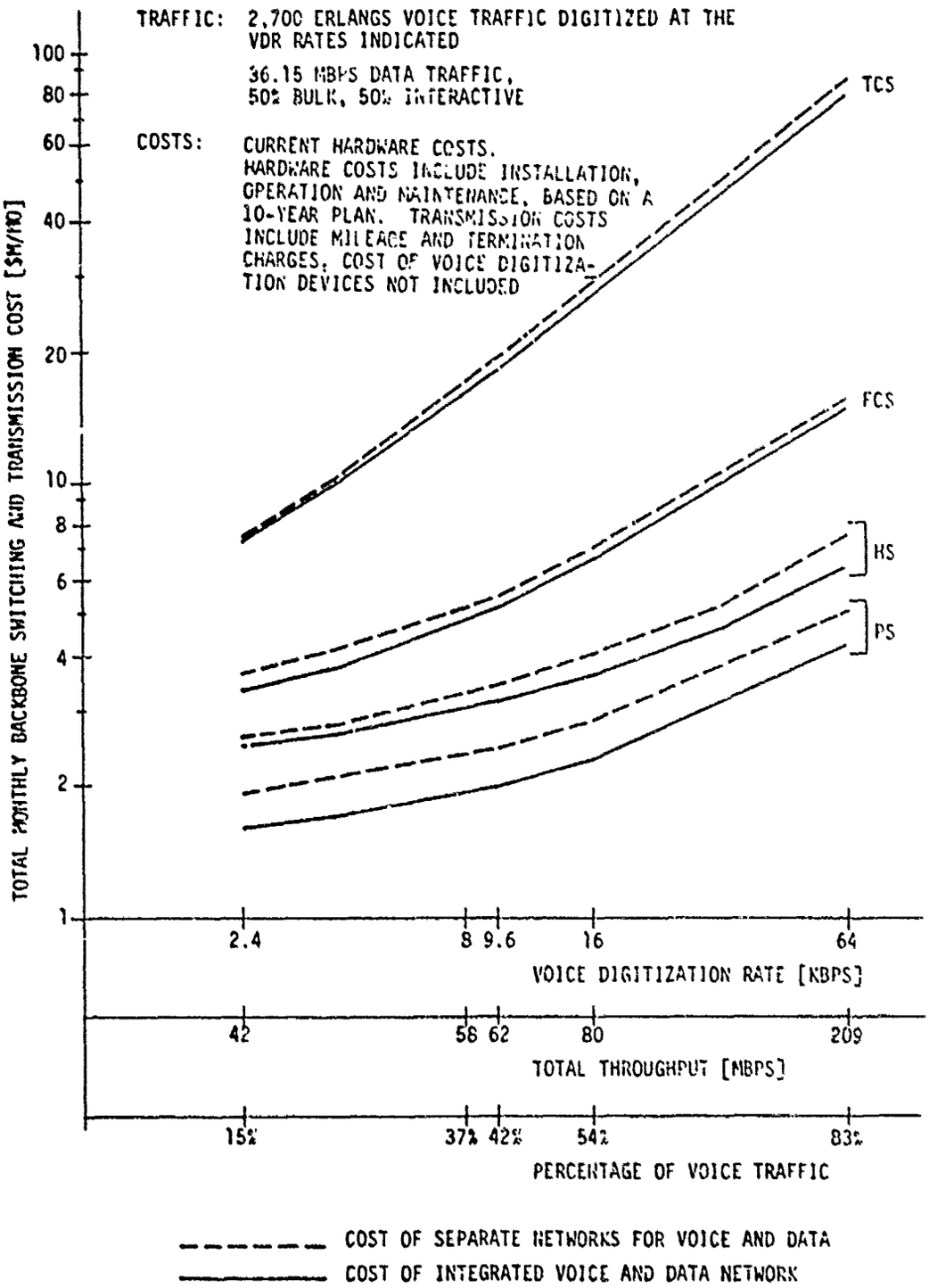


Fig. 2.2 Integrated versus segregated voice and data networks as a function of voice digitization rate (VDR) and switching technology (TCS - traditional circuit switching; FCS - fast circuit switching; HS - hybrid circuit switching; PS - packet switching).

3. voice is digitized at subscriber hand-sets.

The network is designed for the following performance values:

1. 1% end-to-end blocking for circuit switched voice,
2. 200 msec end-to-end packet delay for interactive data users and packet voice, and
3. 600 msec end-to-end packet delay for bulk data applications.

Existing computer and communications costs are utilized to arrive at the cost models for the communication lines and the hardware cost. The communication cost model is given by:

$$LC(i) = 0.61[40.05 + D(i)^{0.873}]\ C(i)^{0.728}$$

where LC(i) = total monthly cost for link i [$/month], D(i) = length of link i (miles), and C(i) = channel capacity of link i [Kbps].

The hardware cost model is a function of processing, memory size and the cost of channel interface. The cost function can be given as

$$SC(i) = 0.35P(i)^{0.65} + 0.3M(i)^{0.9} + \sum_j b_j\ C_i(j)$$

where SC(i) = total cost of switch i [$], P(i) = processing capacity of switch i [10^6 instructions/sec], M(i) = memory size [10^6 (32 bit) words], and $C_i(j)$ = channel capacity of outgoing link.

The parameter b_j represents the cost of the channel interface and is a function of the channel capacity.

3. Cost Comparison of Switching Technologies

The total monthly cost in millions of dollars for various switching technologies as a function of the Voice Digitation Rate (VDR) is shown in Fig. 7.3. The VDR is seen to be an important factor affecting the cost.

For circuit switching, a delay of 140 msec is assumed for circuit setup/disconnection while the duty cycle of an interactive user is assumed to be 10 seconds idle time followed by 1000 bits of an average message.

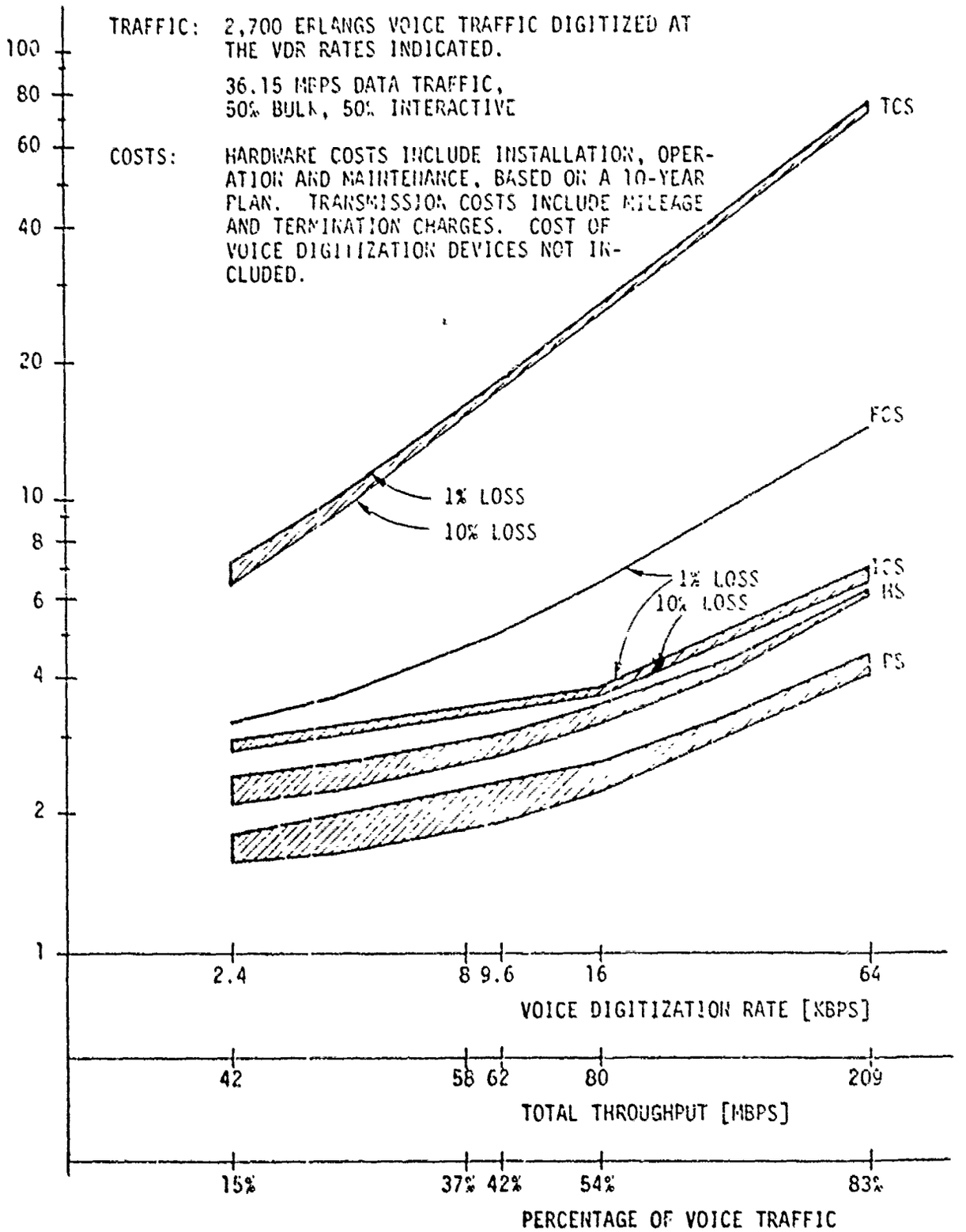


Fig. 2,3 Monthly backbone switching and transmission cost as a function of voice digitization rate (VDR) and switching technology (TCS - traditional circuit switching; FCS - fast circuit switching; ICS - ideal circuit switching; HS - hybrid switching; PS - packet switching). Cost ranges indicate alternative operation scenarios (HS and PS) or blocking probability range (TCS, ICS).

In hybrid techniques, the packet size for interactive data is assumed to be 800 bits with 200 msec average end-to-end delay and the bulk data packet is 1200 bits with a delay of 600 msec.

For packet-switching technology, the following were used to obtain the range of the cost:

1. fixed path protocol (FPP) with headers of 48 bits and 96 bits,
2. path independent protocol (PIP) with headers of 152 bits and 256 bits.

Table 2.1 illustrates a cost comparison of various switching strategies considered here.

The switching cost over the VDR range considered varies between:

1. 9-13% for traditional circuit switching,
2. 53-62% for fast circuit switching,
3. 25-55% for hybrid switching, and
4. 27-38% for packet switching.

The unit costs of backbone switching and transmission per megabit of traffic is given in Table 2.2.

The cost of integrated versus two separate voice and data networks as a function of voice digitization rate is shown in Fig. 2.4.

Table 2.3 shows the cost below which it is economical to provide VDR devices in the backbone network and Table 2.4 indicates the total system monthly cost when VDR is located at the hand-set.

Quantitative results of cost/performance studies for each of the alternative network technologies have also been obtained in this report. Variation of cost as a function of the following parameters have been investigated in detail:

1. interactive user duty cycle in circuit-switching technology,
2. think time of interactive users in alternative network technologies,
3. fixed and moveable boundary frame in hybrid switched system,
4. mixes of bulk and interactive data applications, the packet size for bulk data applications and priorities in hybrid switched backbone network,
5. function of voice digitalization rate, data throughput, voice

Table 2.1 Backbone Network Costs*

	VDR = 2.4 Kbps	VDR = 8 Kbps	VDR = 16 Kbps	VDR = 64 Kbps
Traditional Circuit Switching	7.3 $M/mo	16.0 $M/mo	27.0 $M/mo	77.2 $M/mo
Fast Circuit Switching	3.3 $M/mo	4.8 $M/mo	6.6 $M/mo	14.7 $M/mo
Hybrid Switching	2.5 $M/mo	3.0 $M/mo	3.5 $M/mo	6.3 $M/mo
Packet Switching	1.6 $M/mo	1.9 $M/mo	2.3 $M/mo	4.2 $M/mo

*Cost of voice digitization devices if not included.

Table 2.2 Unit Cost of Alternative Network Technologies

Voice Digitization Rate (Kbps)	Cost of Backbone Switching and Transmission per Million Bits (in cents) Network Technology PS	HS	FCS	TCS
2.4	6.0	9.4	12.4	27.5
9.6	5.2	8.0	13.5	47.1
16	4.7	7.1	13.4	54.6
64	3.2	4.8	11.2	58.8

Traffic Scenario: 2,700 Erlangs Voice and 36.15 Mbps Data

Current Price of [illegible]hing and Transmission

PS-Packe[illegible]witching, HS-Hybrid Switching, FCS-Fast Circuit Switching, TCS-Traditional Circuit Switching

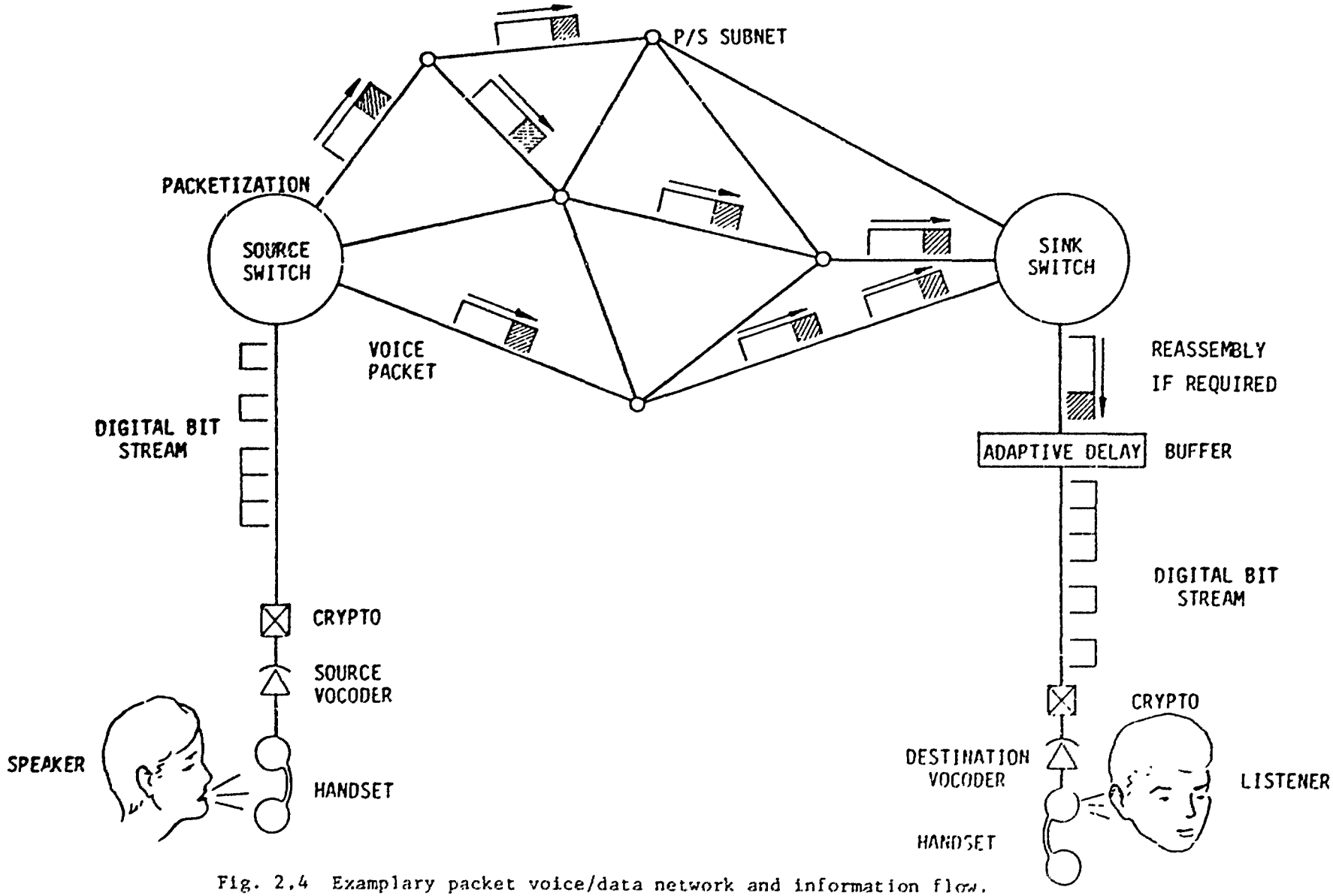


Fig. 2.4 Examplary packet voice/data network and information flow.

Table 2.3 Costs Below Which it is Economical to Provide VDR Devices in the Backbone Network

	2.4 Kbps VDR Device	16 Kbps VDR Device
Traditional Circuit Switching	$98,000	$70,000
Fast Circuit Switching	$16,500	$11,500
Hybrid Switching	$ 5,500	$ 3,900
Packet Switching	$ 3,700	$ 2,800

Table 2.4 Sample Results Comparing Total System Monthly Cost (Backbone Network, Local Distribution Network, Voice Digitization Devices) for the Option of Digitization in the Handset for 100,000 Handsets

	Voice Digitization Rate of 8 Kbps	Voice Digitization Rate of 16 Kbps
Traditional Circuit Switching	$40.8 M/mo	$62.8 M/mo
Fast Circuit Switching	$18.4 M/mo	$22.0 M/mo
Hybrid Switching	$14.8 M/mo	$15.8 M/mo
Packet Switching	$12.6 M/mo	$13.4 M/mo

loss percentage in hybrid switching system,

6. fixed path protocol and path independent protocol in packet switching,
7. impact of composite packet option in packet switching, and
8. voice digitization rate for different data throughput levels in packet switching.

Based on all these results, it is recommended that the packet switching technology is to be selected as the prime alternative for future integrated DOD voice and data networks. But the transition issues from the DOD's current circuit-switched voice network must be investigated and resolved first.

A second alternative is the hybrid switching technique. Development of a network test-bed will be quite useful in all future planning of the network.

4. Discussion

The main shortcoming of this report can be said to be the briefness in developing the study model. The complete analysis and the report is based on the models described in this report. But, step by step explanations are not given regarding the validity of the models.

Another important aspect not well emphasized is the software aspect of the system. The ever-increasing and over-riding cost of software is an important factor in deciding the cost of the present day computing systems. The parallel and distributed processing techniques and the fault-tolerant concepts have created solutions as well as unforeseen new problems. These need special consideration.

CHAPTER III

CARNEGIE-MELLON STUDY OF MULTI-PROCESSOR ARCHITECTURES

1. Introduction

The Carnegie-Mellon report [29] studies the suitability of various multiprocessor architectures for processing integrated data. A multiprocessor system in an abstract form can be represented as shown in Fig. 3.1. The symbols P, M and S represent a processor, a memory unit, and a switch, respectively. Other notations commonly utilized in multiprocessor systems are L for link, K for controller, T for transducer, and D for data operation.

The first system considered in this report is C.mmp (Fig. 3.2) which has a fully-interconnected, central crosspoint switch to connect memory ports to processor ports. The second system (Fig. 3.3) has a fully-interconnected, distributed Processor/Memory switch. Each processor of this Pluribus system may have several processors, each with its own memory. Similarly, each memory module may have several memories. These features reduce the complexity of the interconnection within the switch. The third architecture is Cm* (Fig. 3.4) which has a low concurrency switch (the network of buses) to access the shared memory. The structure is built from Processor-Memory pairs called Computer Modules or CM's. The local memory is also shared in the system. The S_{local} allows the first level of mapping while inter-cluster access is provided by K_{map}. The other two systems included are the Global Bus System (Fig. 3.5) with single cluster of P-M modules and the Tandem multiprocessor structure (Fig. 3.6) with looser interconnections. Access to nonlocal memory in tendem system requires communication between the source and destination processors.

The following sections describe the performance evaluation and reliability, and life cycle cost analysis of the above mentioned five architectures.

2. Performance Evaluation

Processing of integrated voice and data at each node requires several processes and is given in Fig. 3.7. But the decomposition

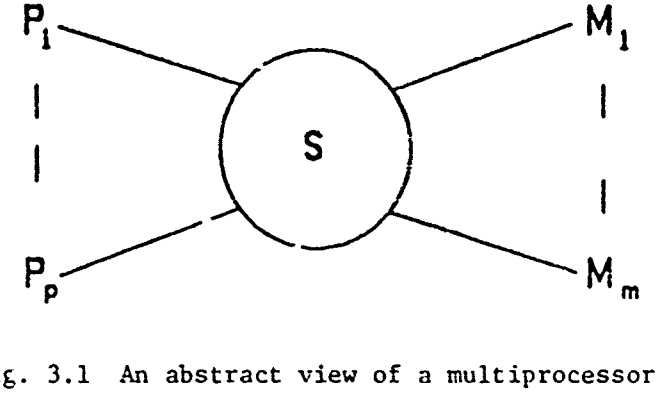


Fig. 3.1 An abstract view of a multiprocessor

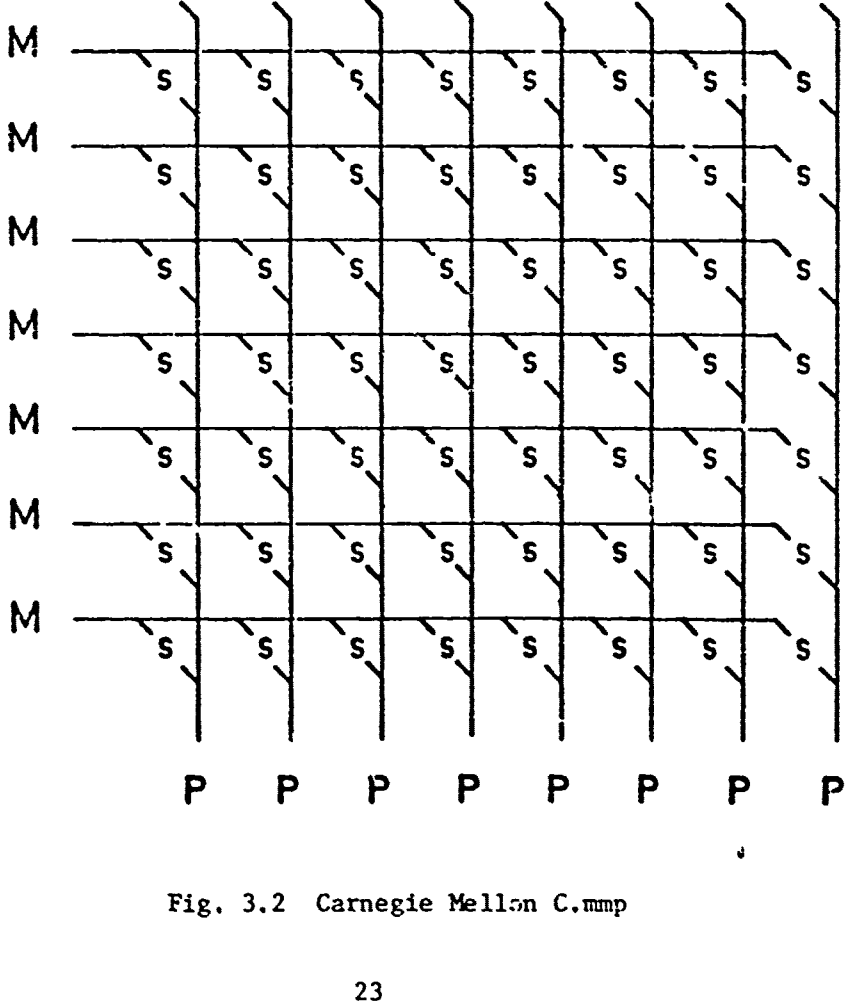


Fig. 3.2 Carnegie Mellon C.mmp

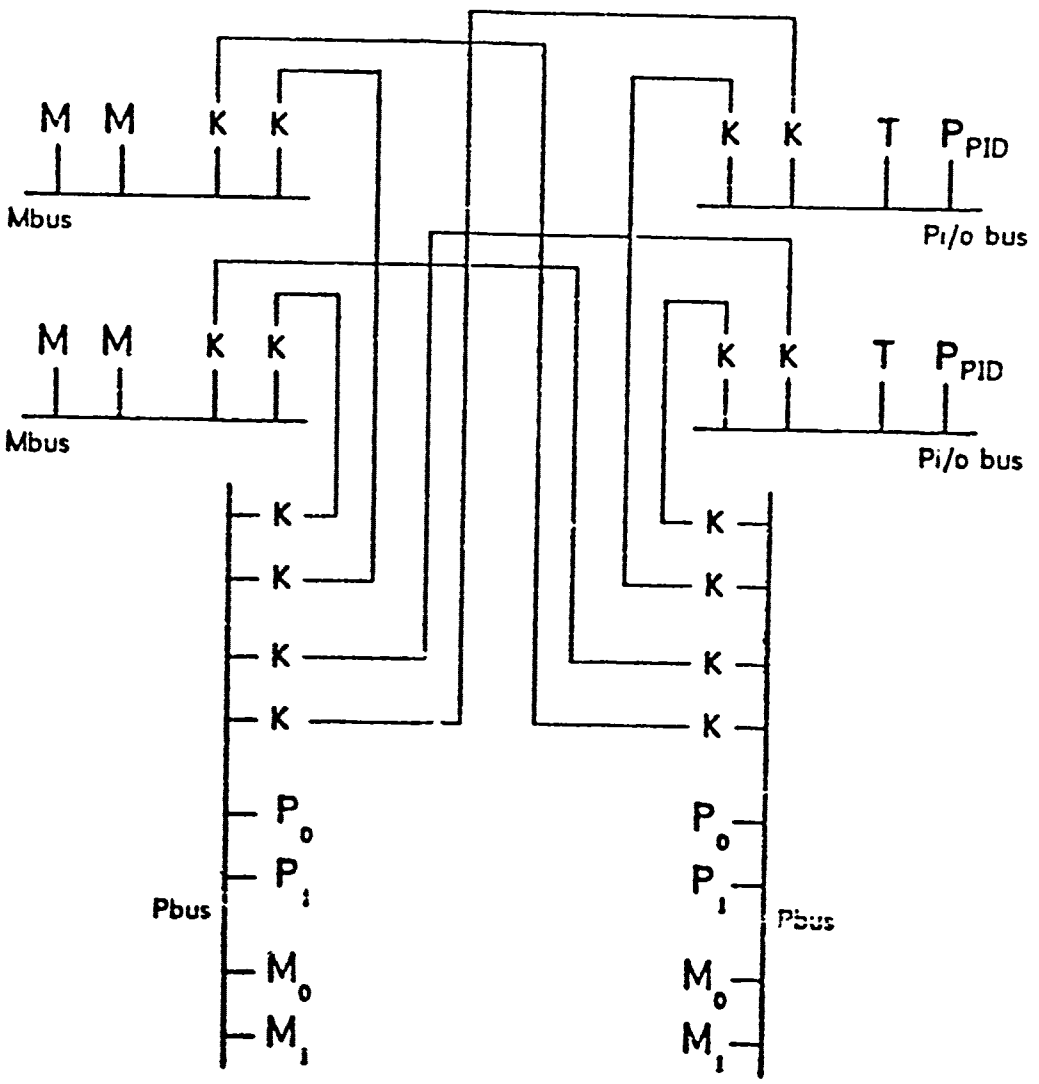


Fig. 3.3 Pluribus system

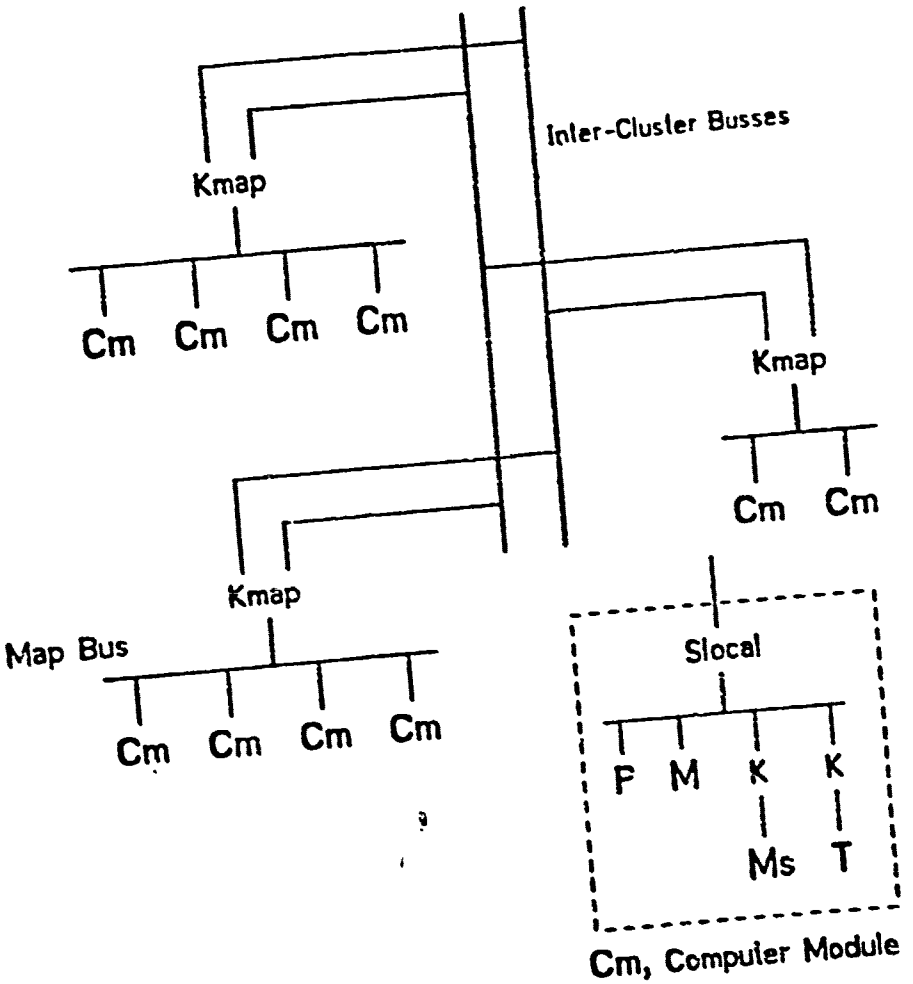
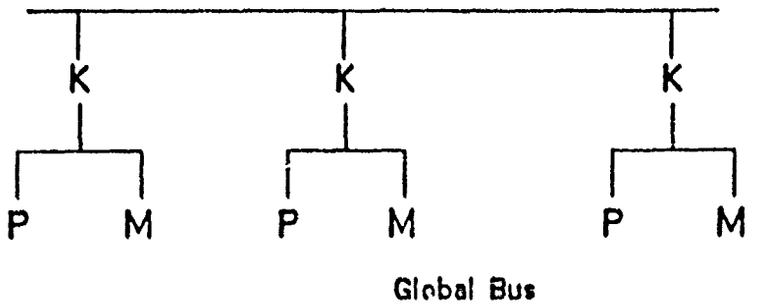


Fig. 3.4 Carnegie Mellon Cm*



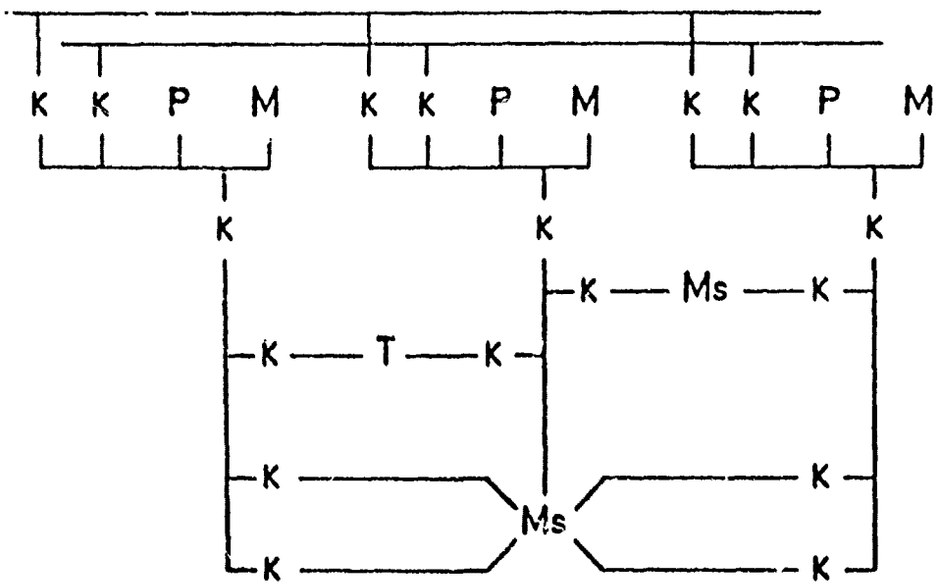


Fig. 3.6 Tandem System

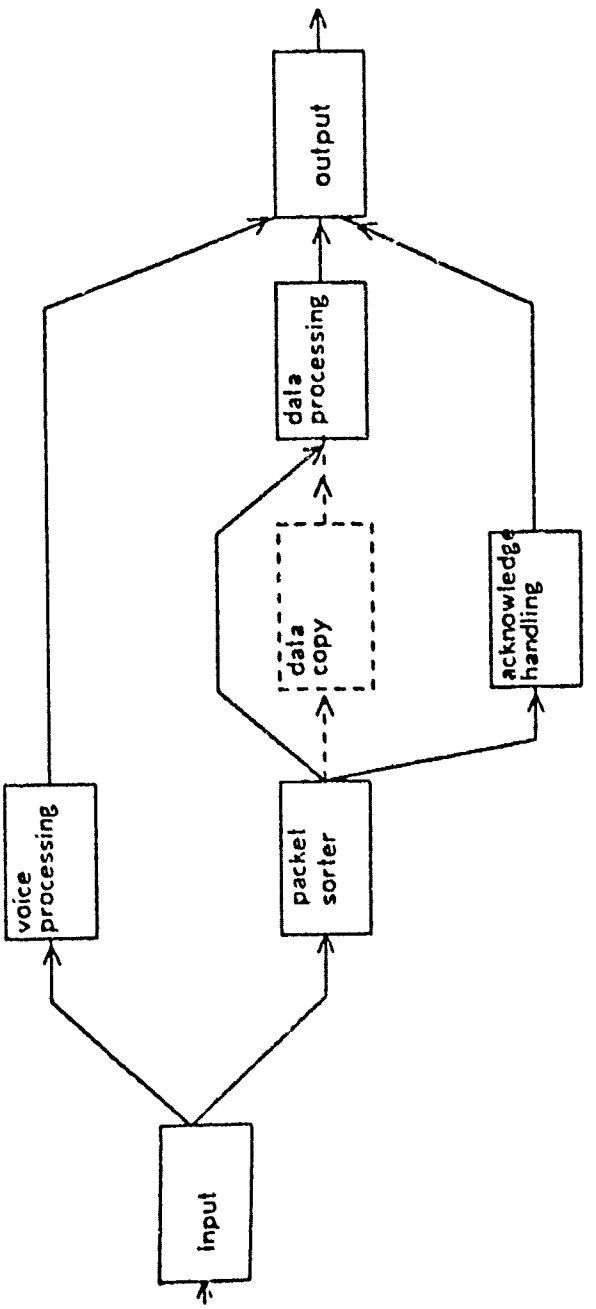


Fig. 3.7 Process identification

into independent tasks itself is a problem and there exists no general solution. Hence, here, two types of decomposition are considered which represent two extreme points in the possible number of combinations:

A. Decomposition I - A processor can execute any task

B. Decomposition II - A processor is dedicated to a particular task.

The communication among the task is assumed to be done through queue of messages. Such queues are stored in the global memory in the case of Decomposition I while Decomposition II requires use of the processor's own local memory for its correspondi g queue.

An example of a decomposition for C.mmp, Decomposition I is given. Each of the three communication lines has the packets as shown in Table 3.1. The total number of memory references for each process to each of the memories and the total time delay is goven in Table 3.2.

The minimum number of processors needed to handle the varying amount of traffic and the two possible decompositions are given in Tables 3.3 - 3.5. The effect of 10 times faster processor and memory units are included in Tables 3.7 - 3.10.

From these tables, it can be easily seen that the C.mmp and Pluribus architectures are best suited for processing the integrated voice and data. This can be easily attributed to their interconnection schemes for the shared memory.

3. Reliability and Life Cycle Cost Modeling

To calculate the reliability and mean time to failures of the various interconnection structures, a computer program has been developed. The input to be defined is the type of architecture, the number of available resources and the minimum number of required modules for the whole system to function (fail-soft).

Figures 3.8 and 3.9 show the C.mmp system reliability for various numbers of required processors and for different sizes of memory modules. Such curves for the Pluribus system are shown in Figs. 3.10 and 3.11. Figures 3.12 and 3.13 indicate the reliability Cm* while Figs. 3.14 and 3.15 are for the Global Bus system. Finally, Figs. 3.16 and 3.17 provide such curves for the Tandem system.

It is well known that the five architectures had differing design goals. C.mmp was meant to be a high performance multi-minicomputer. Cm* was designed to be a highly available, extensible and modular multi-

Table 3.1 Amount of Traffic in Each Communication Line

18 voice slots of three 16 bit words each

18 voice slots of five 16 bit words each

2 data packets of 25 16 bit words each

2 data packets of eight 16 bit words each

6 control packets of four 16 bit words each

Table 3.2 Memory References for Various Processes

Process	No. of Local References	No. of Global References	No. of I/O References	Processing Time (msec)
Voice Processing	12879	2118	3	60000
Packet Sorter	2898	435	63	13584
Data Copy	-	-	-	-
Data Processing	3612	564	48	16896
Acknowledge Handling	2628	432	18	12456
Total	22017	3549	132	102936

Table 3.3 Minimum Number of Processors Needed for 62% Voice and 28% Data Traffic with Decomposition I

Architecture	% of T1 carrier in each of the lines			
	12%	24%	48%	61%
C.mmp	7	12	22	27
Pluribus	7	12	23	29
Global	9	17	31	39
Cm* block move	12	18	33	42
Tandem	-	-	-	-
Cm*	12	21	39	45

Table 3.4 Minimum Requirements for 62% Voice, 28% Data, Decomposition II

Architecture	% of T1 carrier in each of the lines			
	12%	24%	48%	61%
c.mmp	8	13	23	29
Pluribus	9	14	24	30
Global	11	18	32	41
Cm* block move	21	24	39	48
Tandem	-	-	-	-
Cm*	21	27	42	51

Table 3.5 Minimum Requirements for 25% Voice, 67% Data, Decomposition I

Architecture	% of T1 carrier in each of the lines			
	17%	33%	50%	66%
C.mmp	6	9	13	17
Pluribus	6	10	14	18
Global	8	14	21	27
Cm* block move	12	18	24	30
Tandem	-	-	-	-
Cm* -	12	18	27	33

Table 3.6 Minimum Requirements for 25% Voice, 67% Data, Decomposition II

Architecture	% of T1 carrier in each of the lines			
	17%	33%	50%	66%
C.mmp	6	11	14	18
Pluribus	6	11	16	19
Global	9	16	23	28
Cm* block move	18	21	27	33
Tandem	-	-	-	-
Cm*	18	24	30	39

Table 3.7 Minimum Number of Processors Required for 62% Voice, 28% Data with Decomposition I and 10 Times Faster Memory and Processor

Architecture	% of T1 carrier in each of the lines			
	12%	24%	48%	61%
C.mmp	3	3	5	6
Pluribus	3	4	7	8
Global	3	5	9	11
Cm* block move	6	9	12	15
Tandem	6	7	-	-
Cm*	6	9	15	18

Table 3.8 Minimum Requirements for 62% Voice, 28% Data, Decomposition II, 10 Times Faster Processor and Memory

Architecture	% of T1 carrier in each of the lines			
	12%	24%	48%	61%
C.mmp	5	6	7	7
Pluribus	5	6	7	9
Global	7	8	10	13
Cm* block move	18	18	21	21
Tandem	8	9	-	-
Cm*	18	21	24	24

Table 3.9 Minimum Requirements for 25% Voice, 67% Data, Decomposition I, 10 Times Faster Processor and Memory

Architecture	% of T1 carrier in each of the lines			
	17%	33%	50%	66%
C.mmp	2	3	4	4
Pluribus	3	3	4	5
Global	3	5	7	8
Cm* block move	6	9	9	12
Tandem	6	8	-	-
Cm*	6	9	12	15

Table 3.10 Minimum Requirements for 25% Voice, 67% Data, Decomposition II, 10 Times Faster Processor and Memory

Architecture	% of T1 carrier in each line			
	17%	33%	50%	66%
C.mmp	5	5	5	6
Pluribus	5	5	6	6
Global	6	7	8	9
Cm* block move	18	18	18	18
Tendem	9	9	-	-
Cm*	18	18	21	24

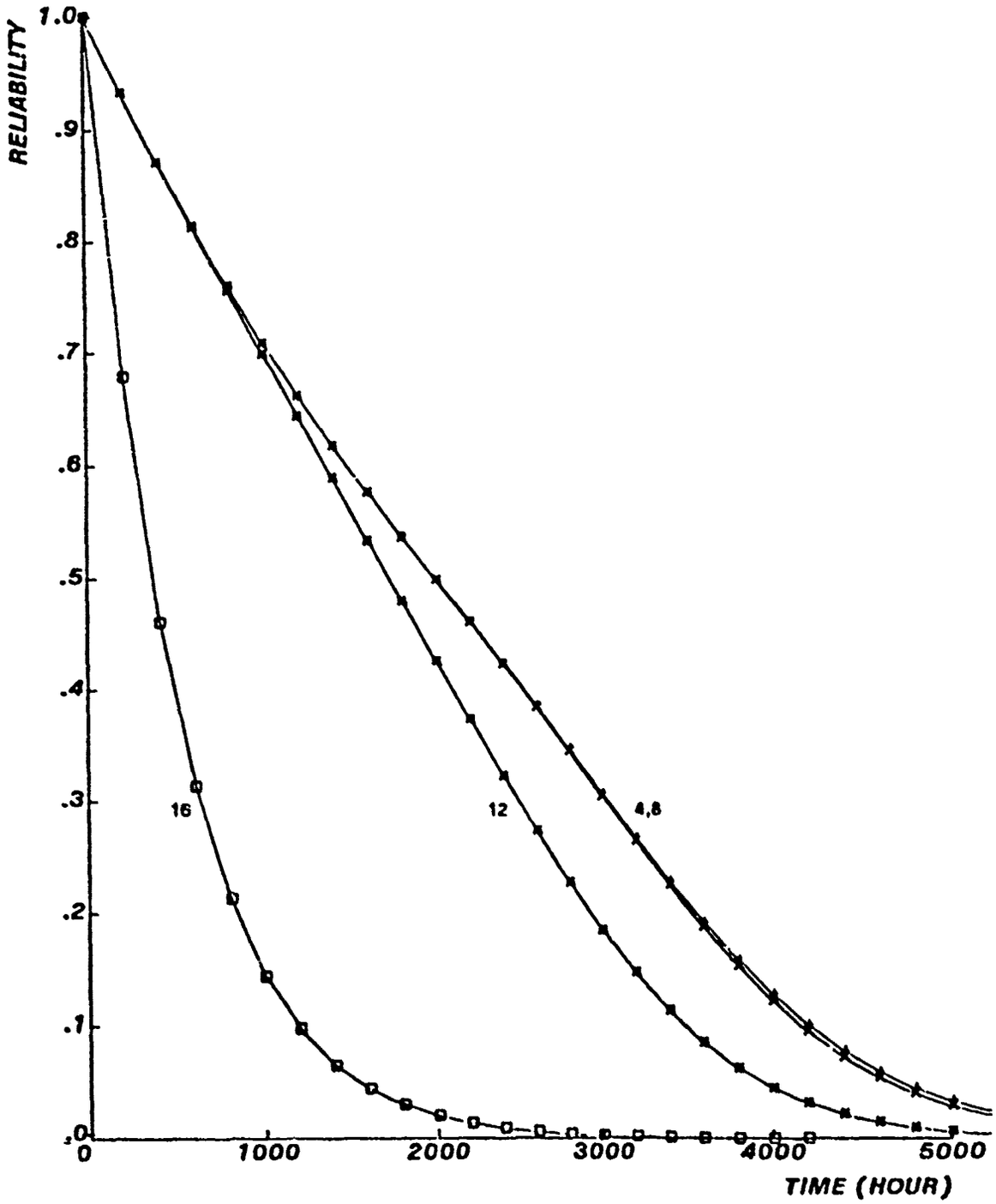


Fig. 3.8 C.mmp with 64Kw per port, 512Kw required (lumped switch)

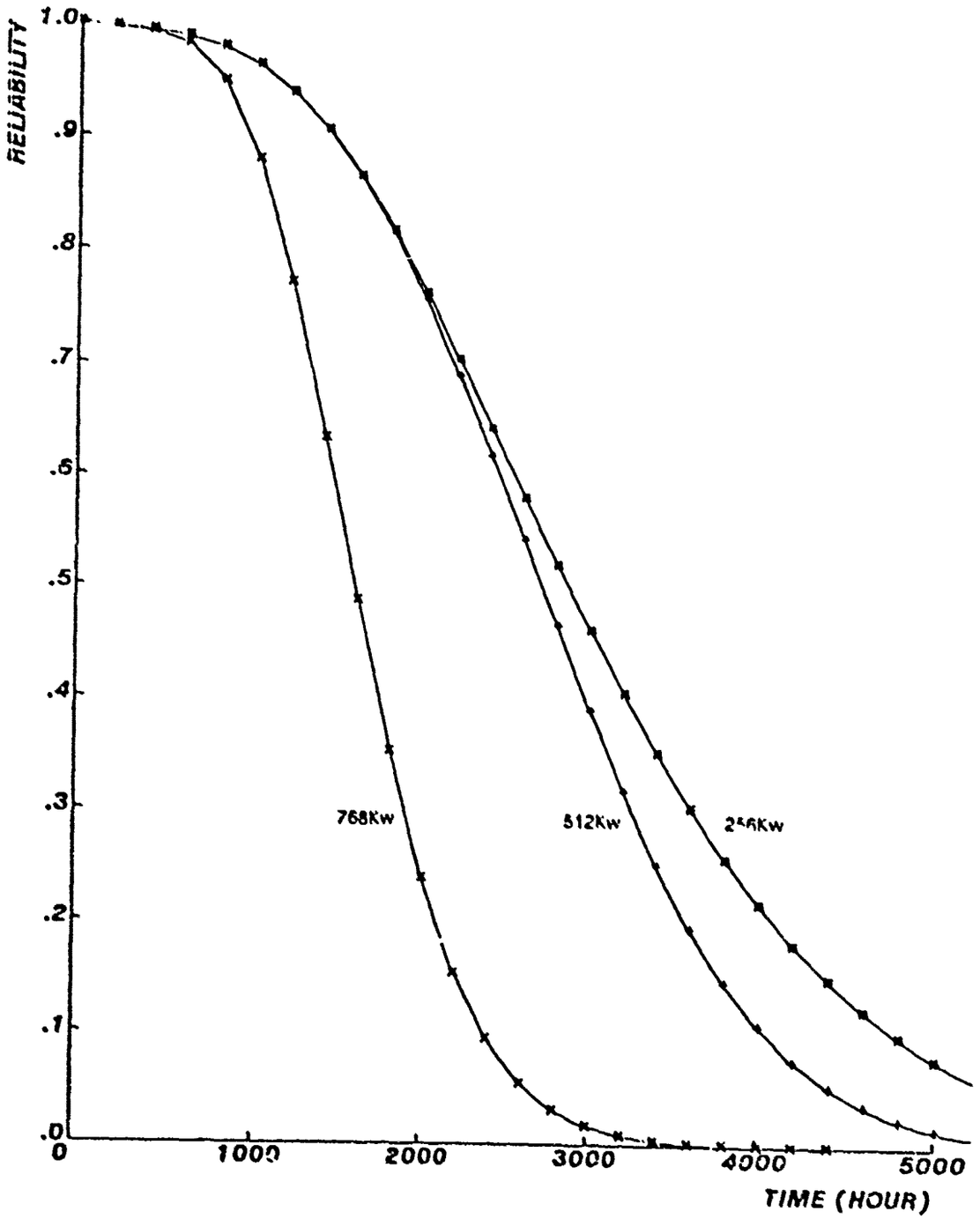


Fig. 3.9 C.mmp with 64Kw per port, 12 processors required (distributed switch)

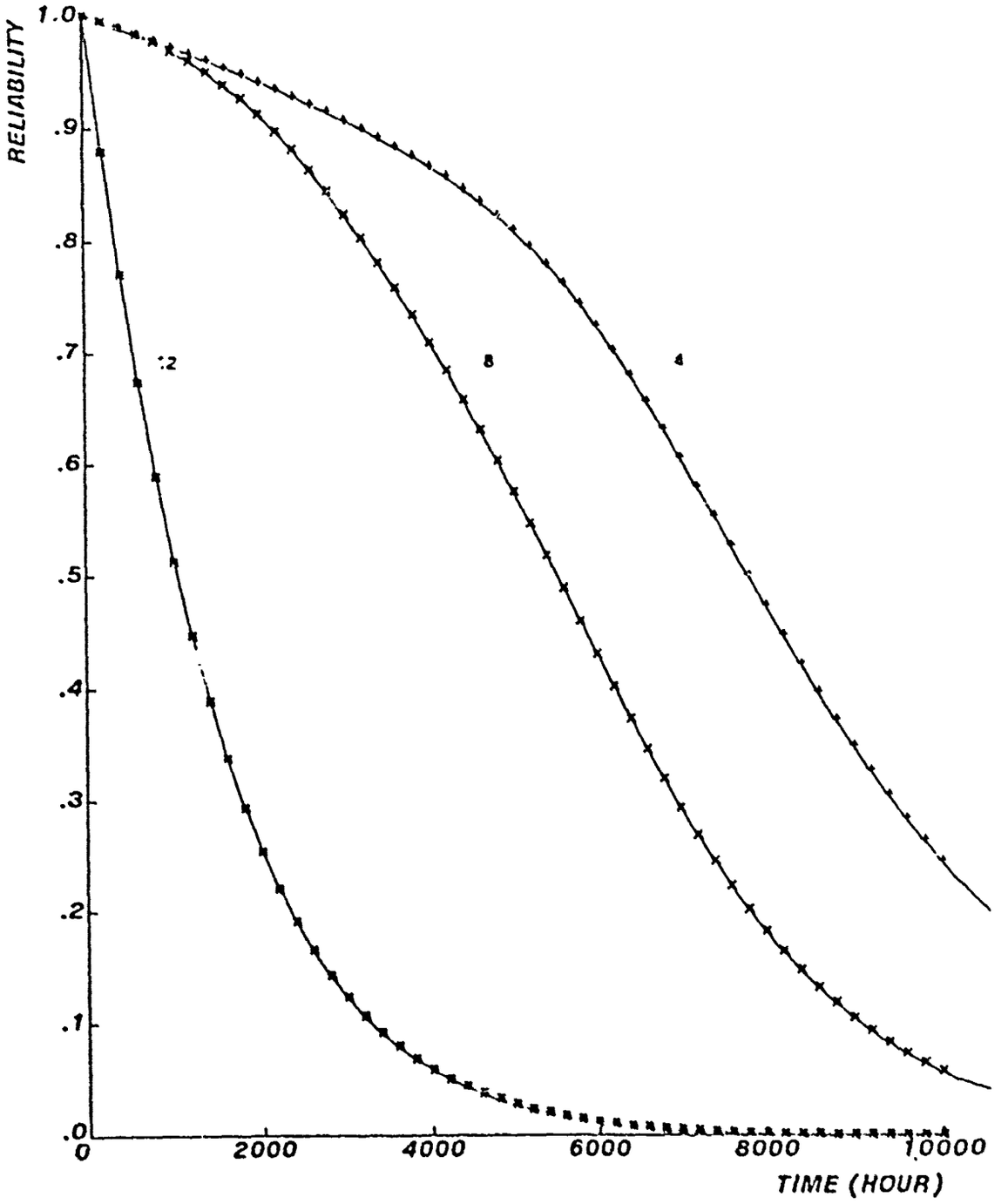


Fig. 3.10 Pluribus with 6 processor buses, 3 memory buses, 128Kw/memory bus, 216Kw required.

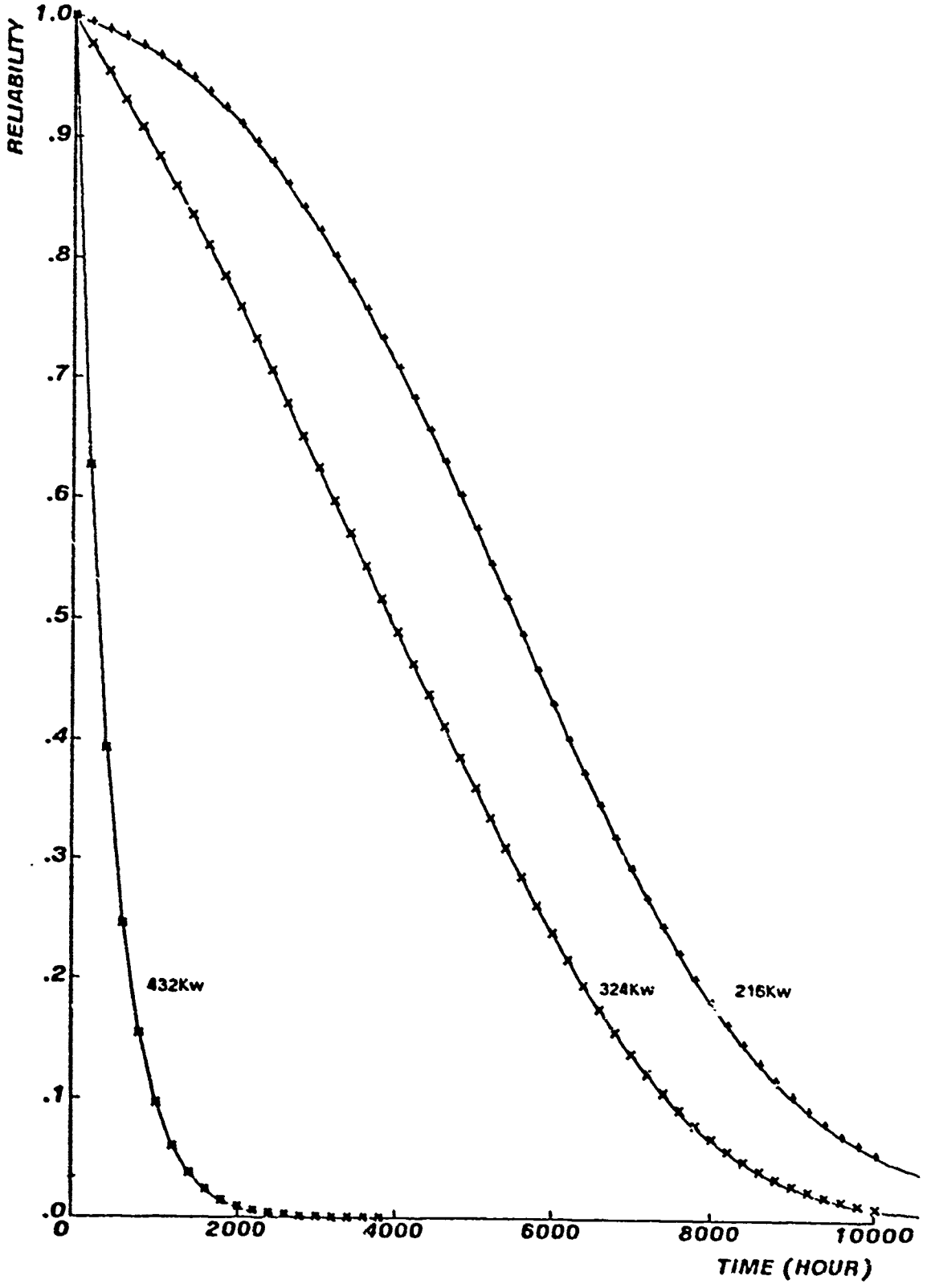


Fig. 3.11 Pluribus with 6 processor buses, 3 memory buses, 128Kw/memory bus, 8 processors required.

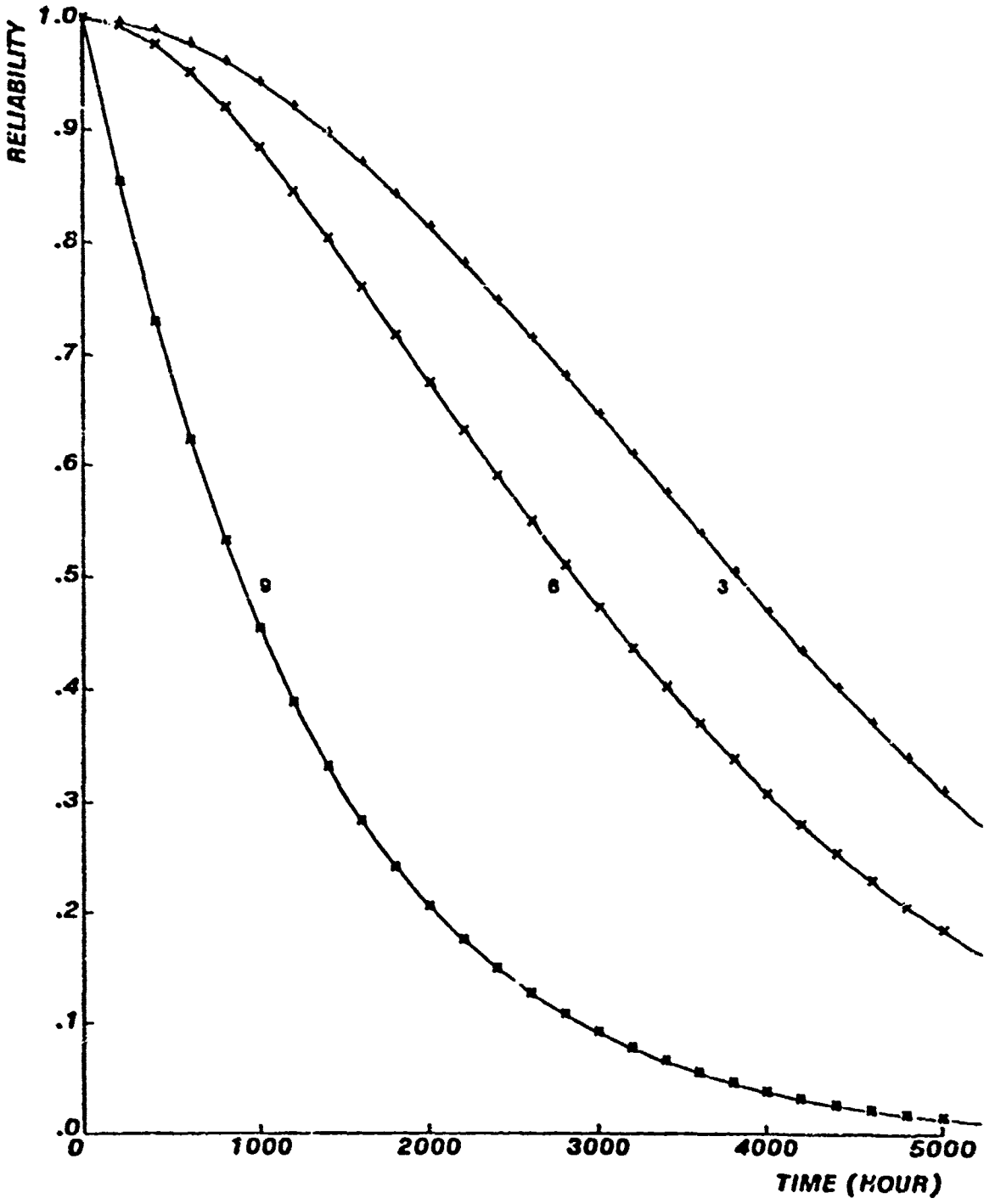


Fig. 3.12 3-Cluster Cm* with
three processors/cluster, 32Kw/Cm, 144Kw required (parallel buses)

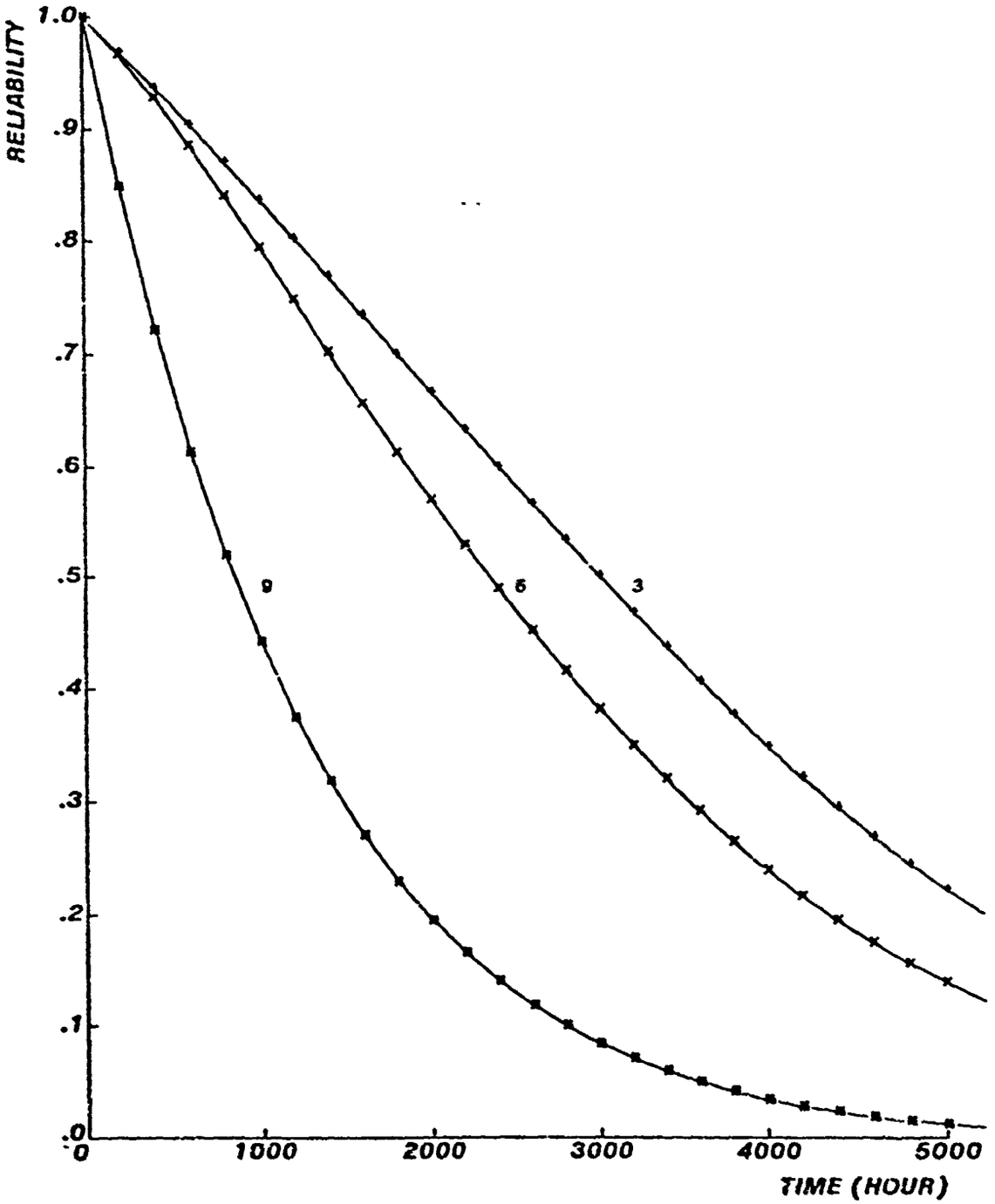


Fig. 3.13 3-Cluster Cm* with three processors/cluster, 32Kw/Cm, 144Kw required (checkerboard)

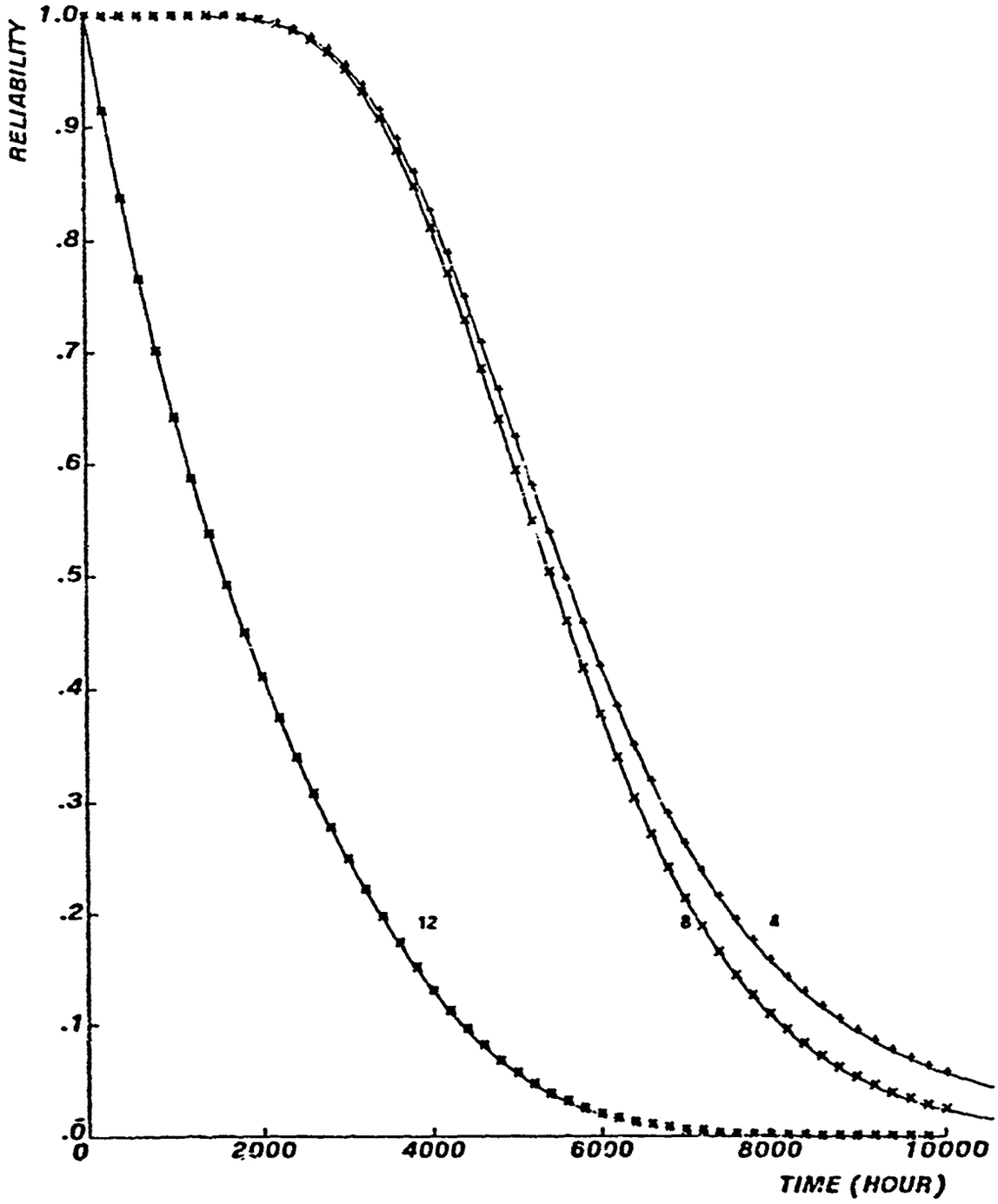


Fig. 3.14 Global bus with 12 processors, 32Kw/processor, 128Kw required

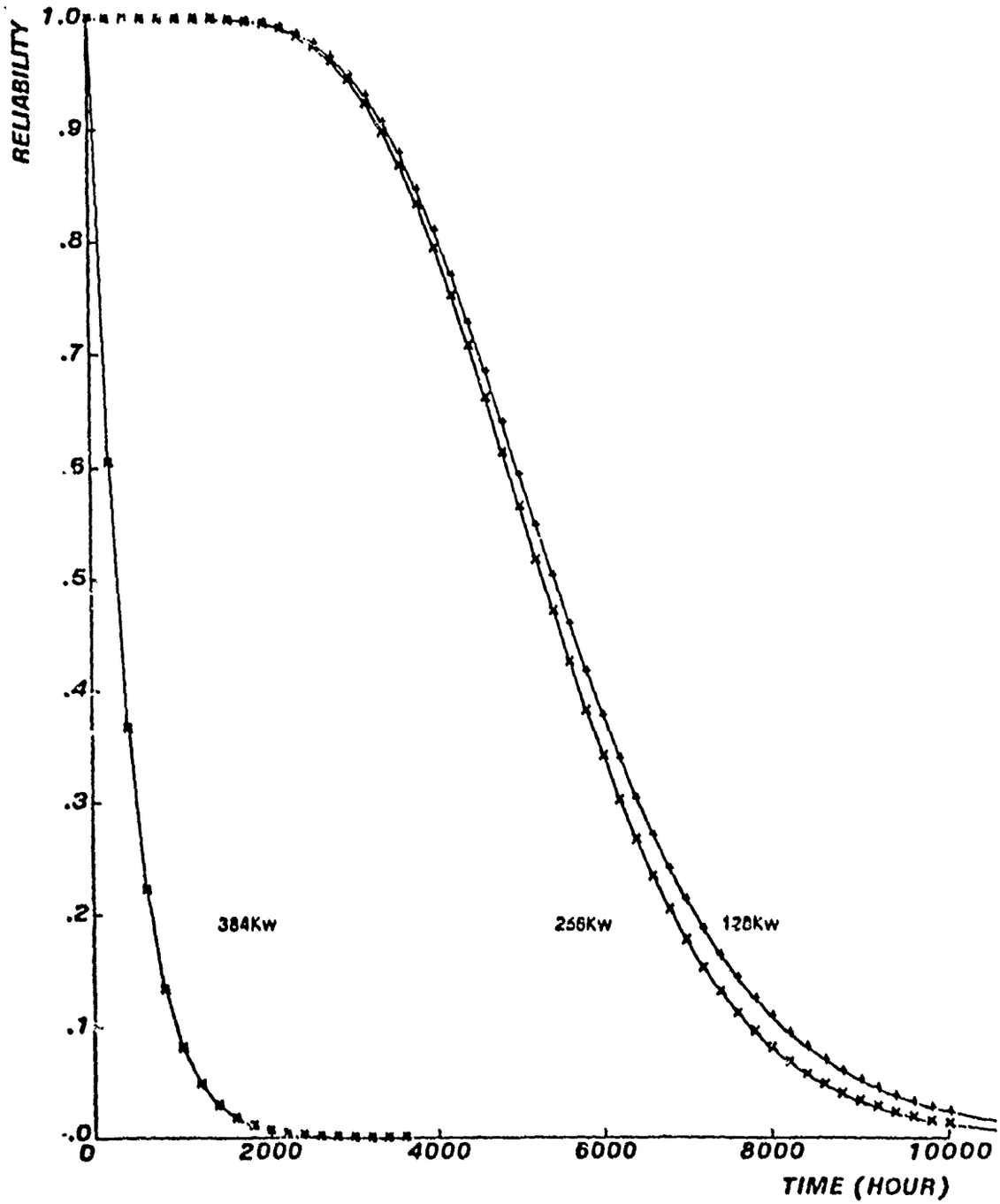


Fig. 3.15 Global bus with 12 processors, 32Kw/processor, 8 processors required

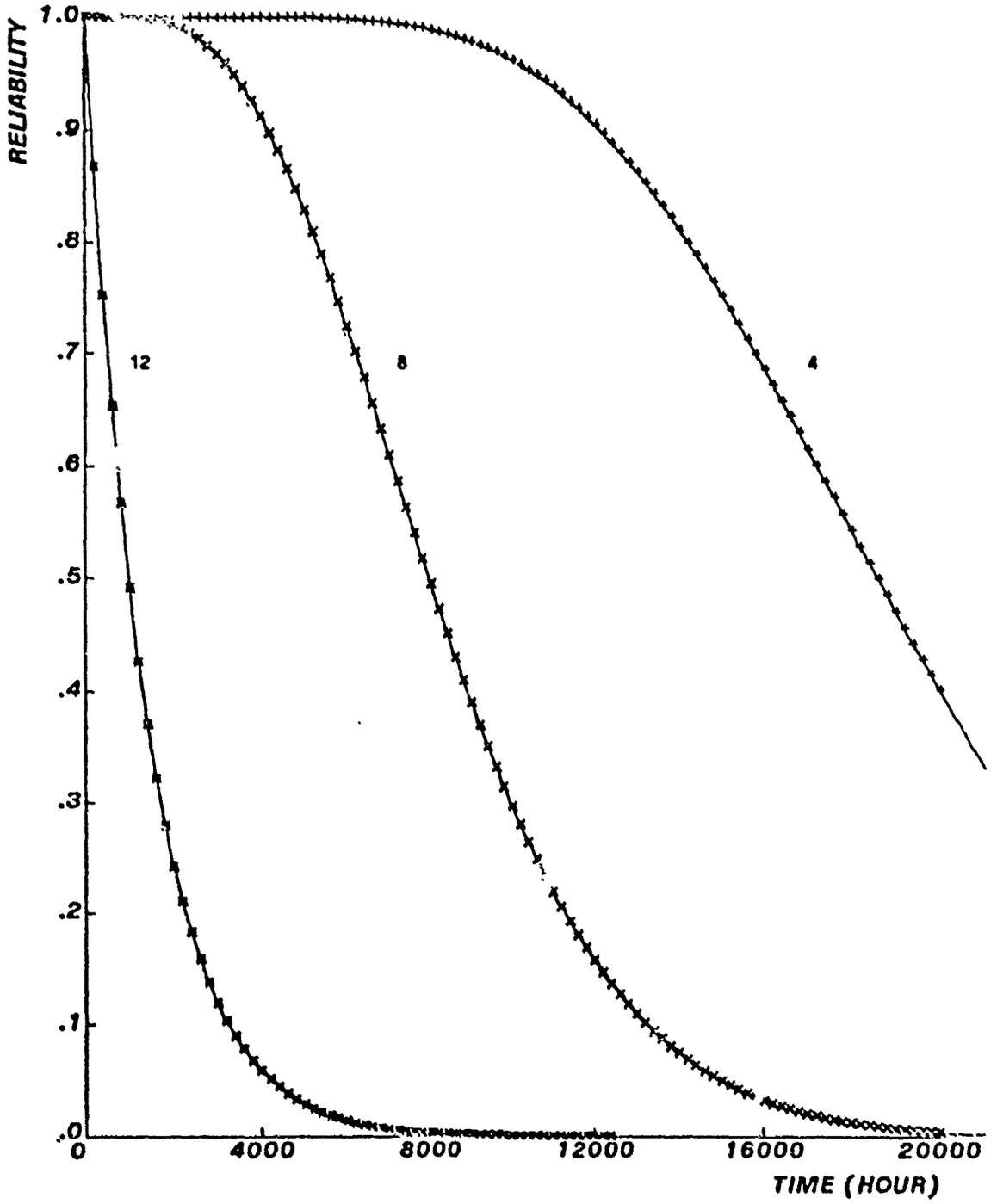


Fig. 3.16 Tandem with 12 processors, 32Kw/processor, 16Kw/processor required.

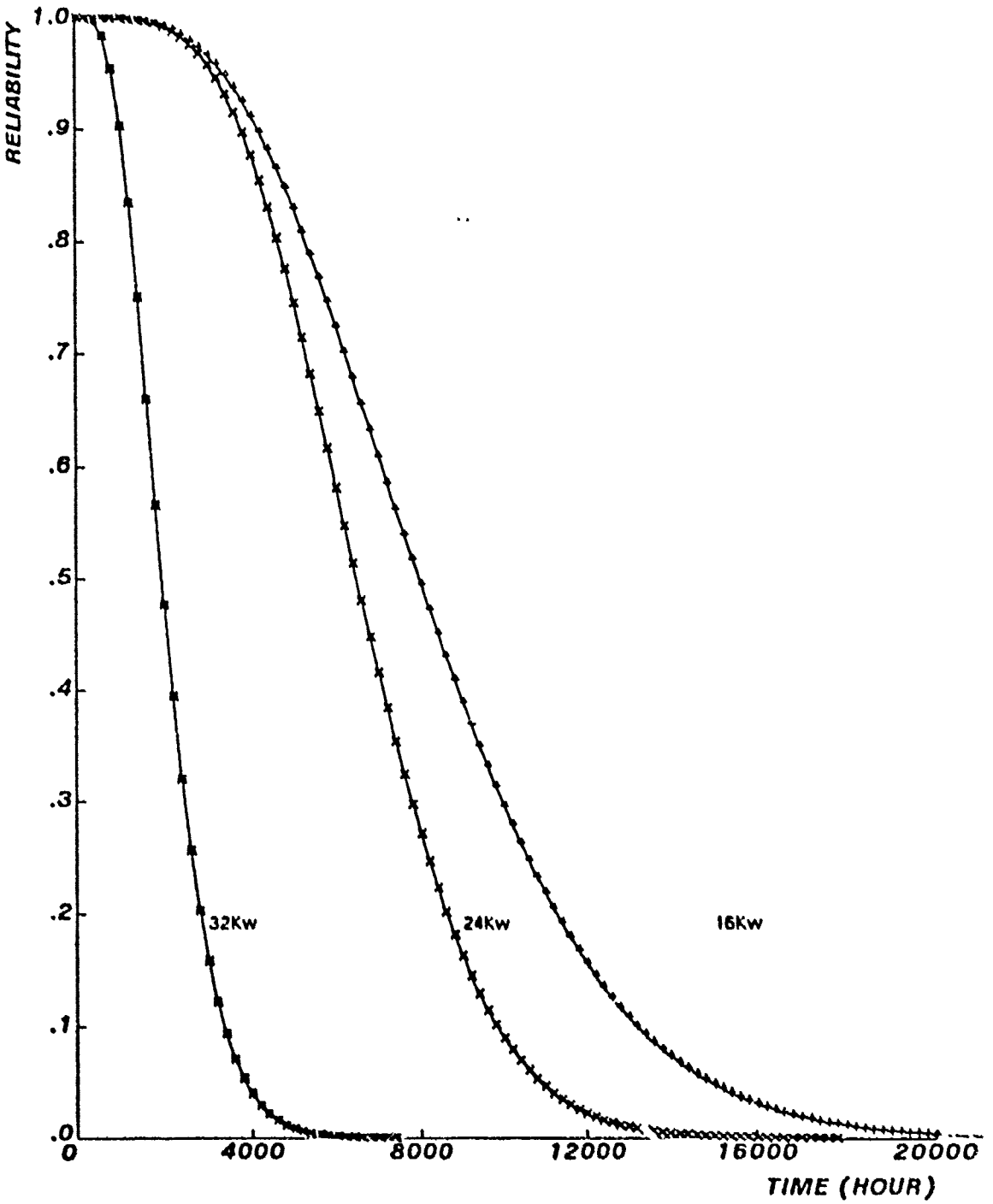


Fig. 3.17 Tandem with 12 processors, 32Kw/processor, 8 processors required

processor. Pluribus and Global were meant to be modular and extensible multiprocessors. Tandem was a highly available multiprocessor. Before we can compare the reliability of the five systems, we have to normalize these architectures with respect to a common factor. Figure 3.18 depicts the reliability curves for these configurations with 12 processors and 384K word memory and shows Pluribus and Global Bus the best. Another way of comparison is to obtain the reliability of these systems with minimal amounts of resources needed for the same performance. Such curves are shown in Figs. 3.19 - 3.21 which indicate C.mmp and Pluribus are best.

4. Conclusion

The use of multi-processor architecture for efficient handling of integrated voice and data at each node seems to be very useful. The multi-processor system not only provides parallel processing capabilities but allows high availability, fault tolerance and graceful degradation. The question of which multi-system structure is to be selected largely depends on the user requirements. One major shortcoming of the Carnegie-Mellon report can be easily identified. All of the five architectures have fixed configuration and there is a need to consider a system having a flexible interconnection network between various functional modules. This growing need has been emphasized by several researchers and this should no longer be neglected.

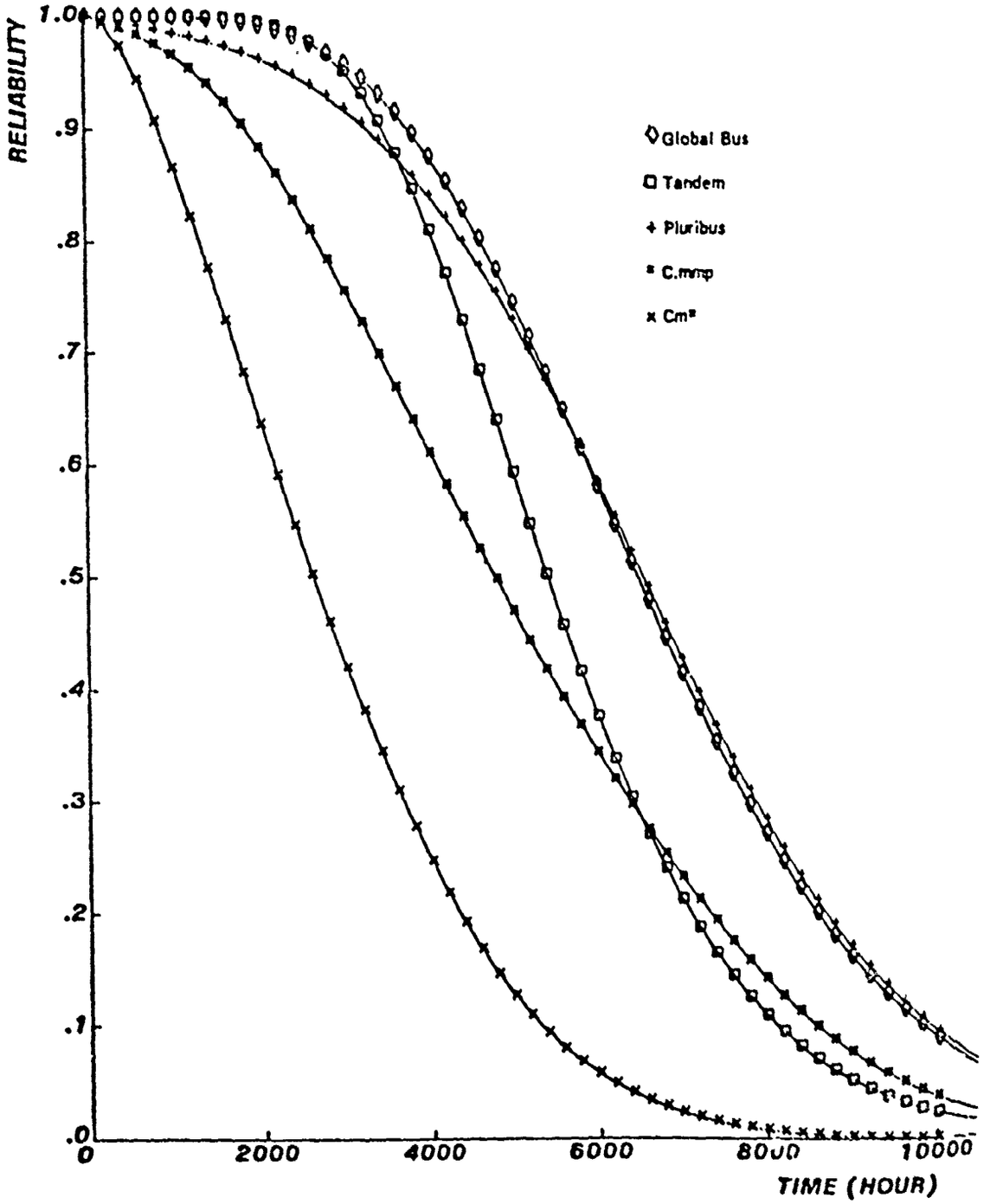


Fig. 3.18 Equivalent number of processors and memory modules

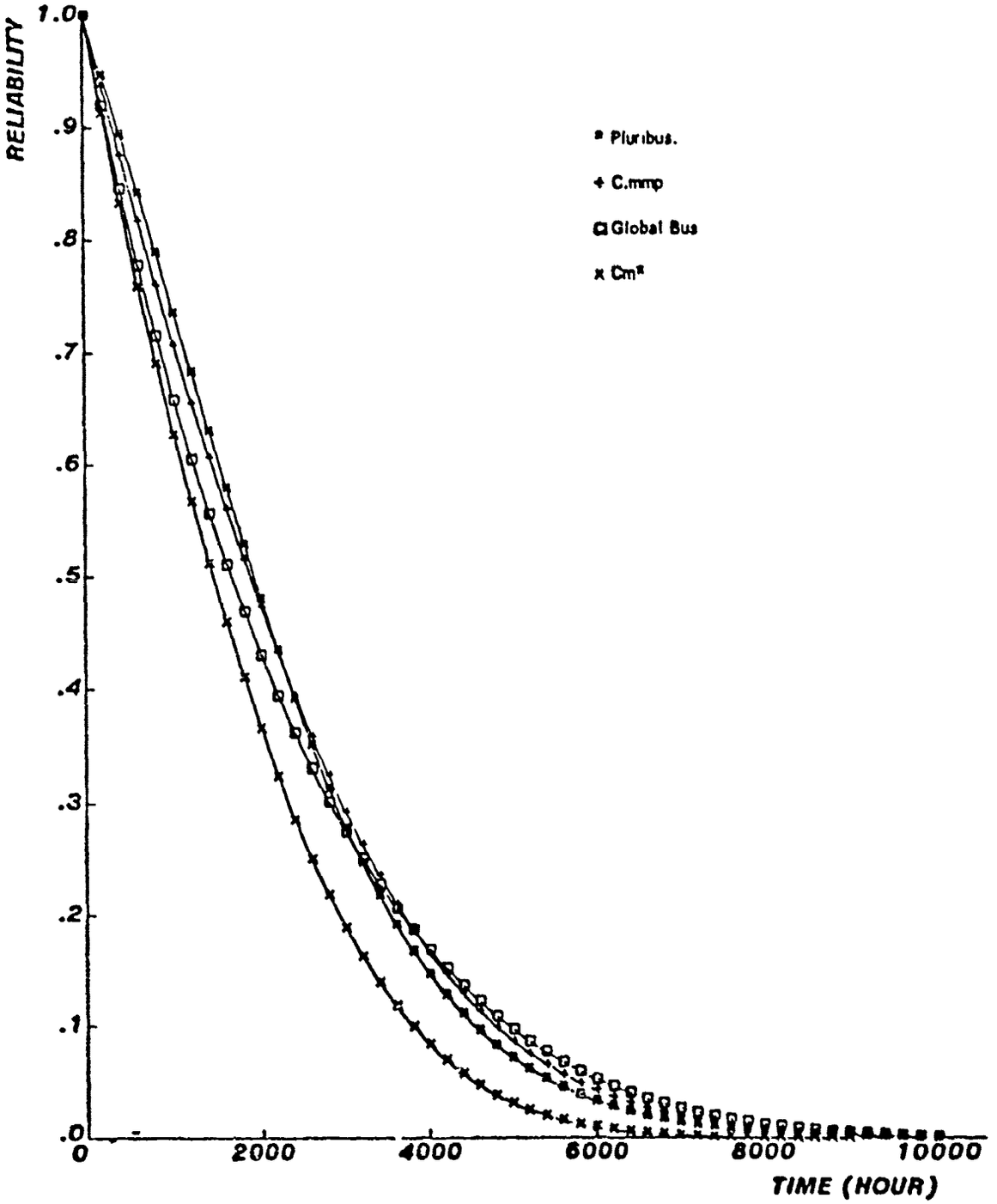


Fig. 3.19 Equivalent performance 62% voice, 28% of data, normal processor, 24% of T1 carrier in each line, three lines

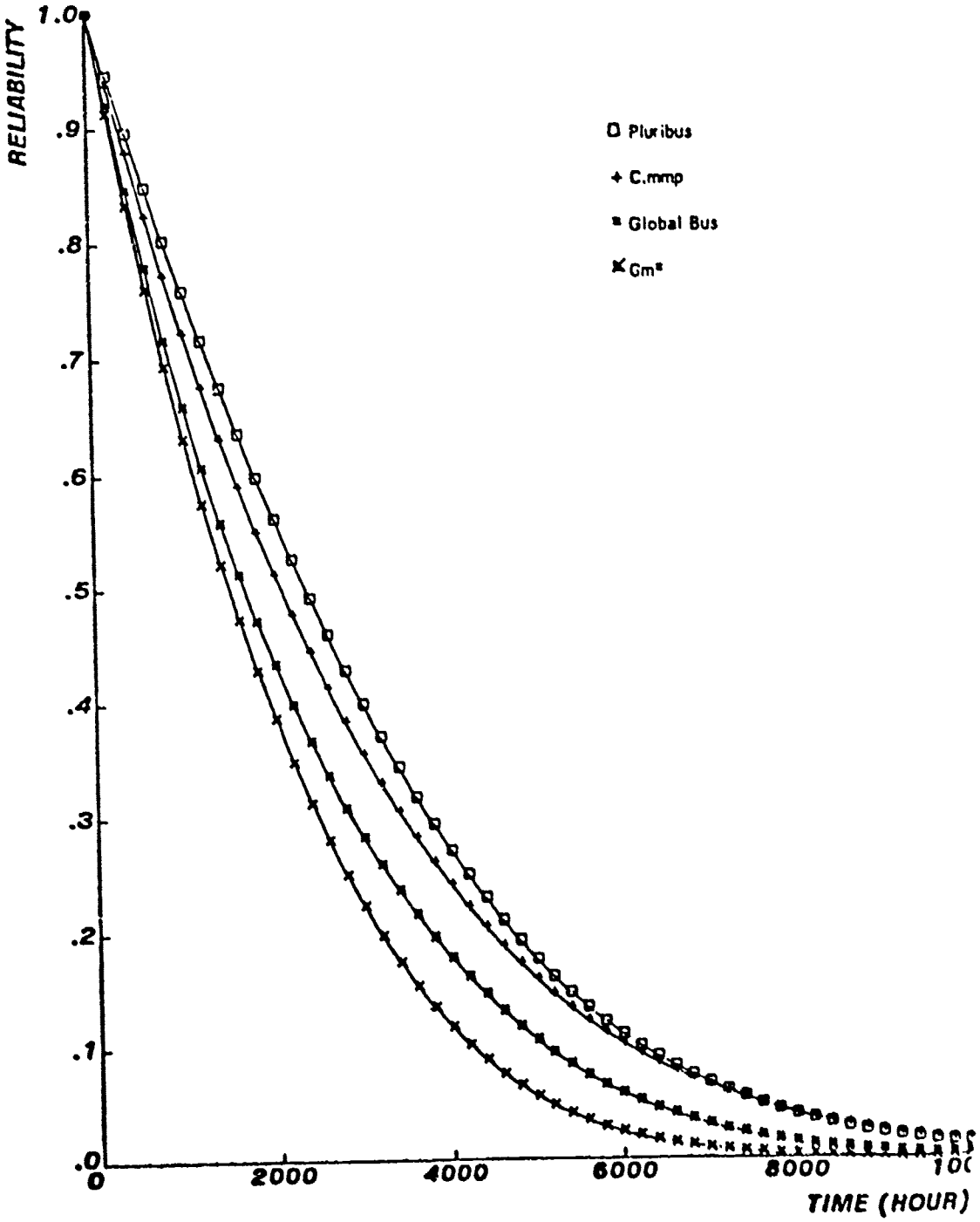


Fig. 3.20 Equivalent performance 62% voice, 28% data, ter times faster processor, 48% of T1 carrier in each line, three lines.

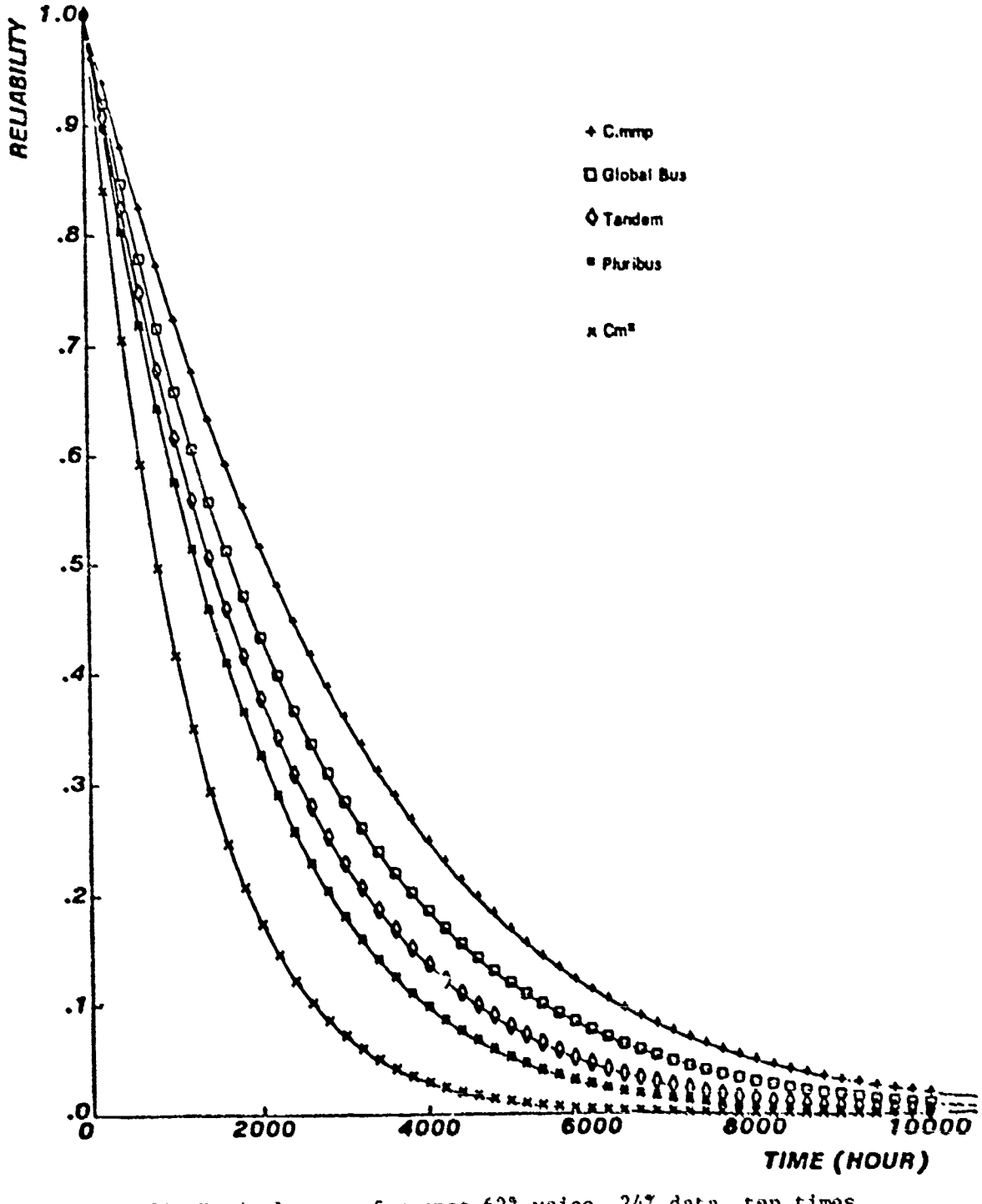


Fig. 3.21 Equivalent performance 62% voice, 24% data, ten times faster processor, 24% of T1 carrier in each line, three lines.

CHAPTER IV

NORTH ELECTRIC COMMUNICATIONS PROCESSOR SYSTEM

1. Introduction

A Communication Processor System (CPS) is usually referred to as the entire array of equipment required to implement a working switching center. The functional baseline of the CPS proposed by the North Electric Company [15] has been derived to suit the requirements of the potential applications such as the Message Switching, Packet Switching, Circuit Switching, Technical Control, Digital Concentrators, etc. The selection of the features to be incorporated is based on their suitability to the present and projected military communication requirements. The major operational considerations for the communication systems include the message accountability, the common channel signaling, the network control and management, and the dynamic trunk allocation techniques.

The message accountability indicates the traffic service reliability of a communication system. The military application requires more rigid processing steps of the message delivery, receipt acknowledgement and the automatic retransmission capacity whenever needed.

The common channel signaling offers several distinct advantages over the presently utilized inband signaling method. This technique allows exchange of information between processor controlled switching systems over a network of signaling links, thereby obtaining increased signal speed and information capacity and an improved reliability associated with increased flexibility.

The network control and management problem is relatively new and additional work in this area will produce continued enhancement in automated control operation.

The dynamic trunk allocation technique as discussed in Chapter IV allows multiplexing of various types of digital traffic so that improved performance can be achieved by an increased usage of the facilities.

All necessary computation requirements are implemented by either using hardware or software. A specific functional allocation to either hardware or software is decided based on its suitability to the

characteristics such as system flexibility and rapid reconfigurability, increased throughput by central processors off-loading, cost-effectiveness and simplicity in system control. For some of the functions, a proper union of the software and hardware provides more effectiveness.

On the hardware design side, the architectural decisions are taken after a careful evaluation of the existing systems. The important questions posed are the selection between monolithic and multi-computer system, the size of the computer, the interconnection topologies between processing units, memory modules and other units of the system and the use of private memory, shared memory, or both private and shared memory. Based on all these factors, the North Electric study led to the architecture of a distributed processor computing system designated as the Central Computing Complex (CCC). The nine specific semi-autonomous units constituting the CCC and their intercommunication path via the connection matrix, are shown in Fig. 4.1. Many attributes of a CPU have been allocated to other units and due advantage of LSI technology has been taken to make the units smart.

Several important factors affect the performance of a computing system. The four sets of objectives characterizing the salient features of the processing system architecture have been recognized as follows [15]:

A. Functional Requirements

The principle functions to be performed by the CCC is to provide high-speed processing associated with the system flexibility and reconfiguration capability. These functions can be classified as:

1. modularity at the unit level,
2. replication as needed at the unit level,
3. automatic graceful degradation and recovery,
4. self-failure detection,
5. built-in diagnostic facilities and commands,
6. built-in monitoring capabilities, and
7. expandability from a minimum set of units.

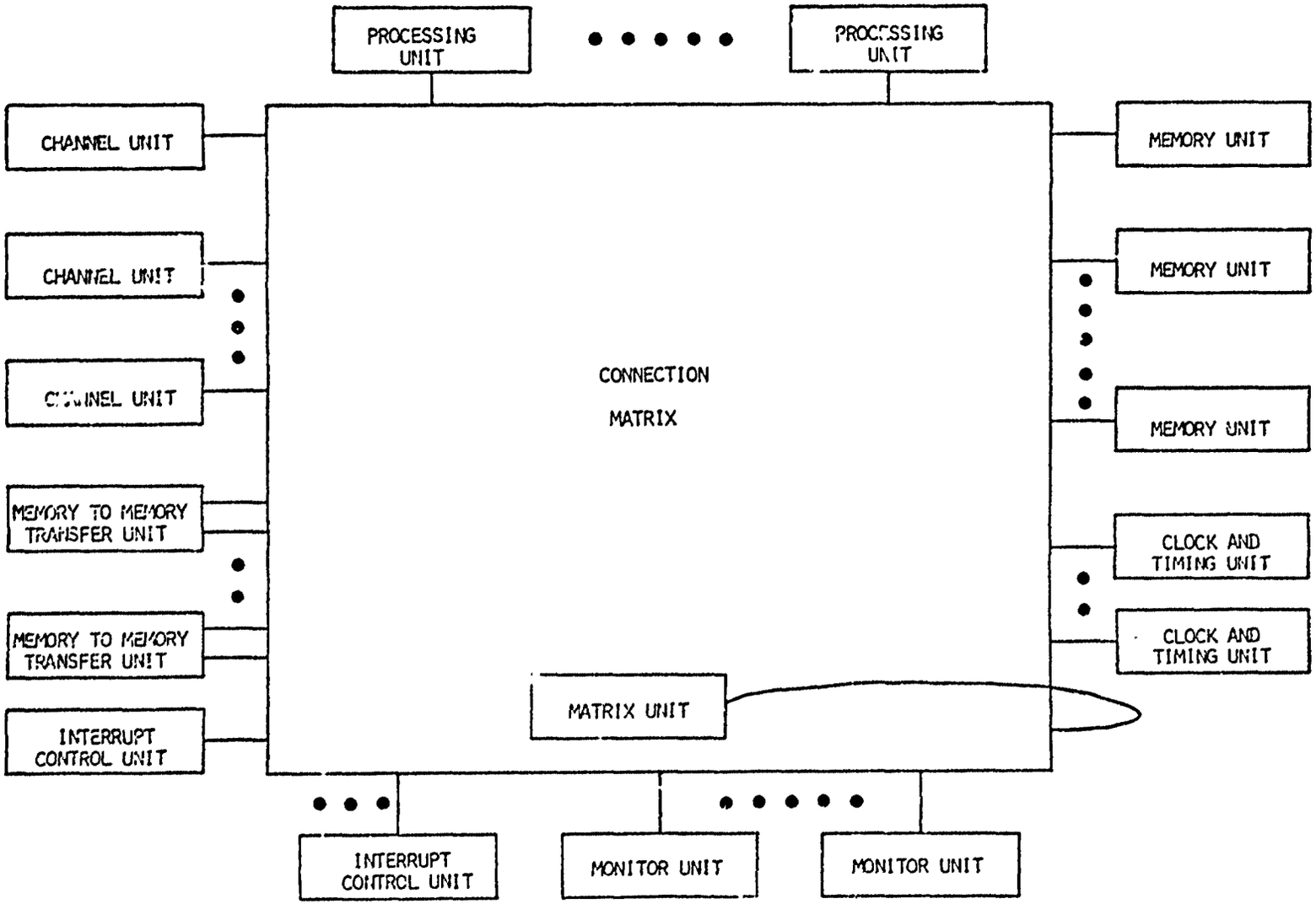


Fig. 4.1 Central computing complex

B. Range of Resource Requirements

The range of necessary support desired for the system gives an idea of the approximate variation of different resources needed for the system. The total working memory, the size of the mass memory, the speed of the instruction execution, the word-length, the power of the repertoire, and the number of channels, etc., reflect the essential information needed for the resource requirements. Normally, a compromise on the selection and the limits of the resources are done in such a way that each of their utilization factors can be optimized in the best possible way.

C. Operational Availability

The Communication Processor System (CPS) requires the availability figure to be as close to 100% as possible. Even the value of 0.996, common in most commercial applications, is not acceptable. Viability requirements are usually satisfied by the replication of the units. Thus the better availability accomplishment encourages the adoption of modularity that provides on-line testing and high diagnostic resolution and isolation of failed units. The solid-state technology has continued to improve the reliability of the digital subsystems and at a certain point of advancement, the inclusion of redundancy may not allow substantial improvement in the overall reliability of the system. Hence, efforts are directed towards minimizing the redundancy cost without any adverse effect on the reliability factory.

D. Architectural Survivability

The architectural survivability of a complex system like CPS is very important. The cost-effectiveness of a system should be considered for the total life-cycle costs and not just the purchase cost. The life-cycle time of 10 to 20 years for a CPS is quite common. The survival of a system is affected by the factors such as the improvements in the component fabrication technology, shift in the applications baseline, the modifications in the digital system design principles, and the changes in the software

support language, etc. The present trends in hardware cost reduction does not seem to be changing in the near future and the dominant parameter of primary concern that governs the cost of a new scheme is the money investment in preparing the necessary software for a totally new system. Hence, much attention is concentrated in simplifying the software design costs and thus reducing the overall cost of the operating system.

2. Architectural Description

The connection matrix unit with inherent graceful degradation capacilities is the heart of the CCC. The modular structured matrix is self-diagnosing and causes interrupt whenever an incorrect connection setup is tried. All the units of the CCC possess the following characteristics.

1. common interface with the matrix and with each other,
2. unit generic micro-instructions,
3. dynamically modifiable logical identity (LID) which can differ from its physical identity,
4. interchangeability with any other unit of the same type,
5. self-failure and malfunction detection,
6. interconnection to other units via the matrix,
7. logically isolation from other units, and
8. power isolation from other units.

The different units of the CCC are essential, inseparable and equally important. In fact, the load of CPU has been reduced by adding a separate Interrupt Control Unit. A maximized size system with up to 254 units might consist of 48 matrix control units, 16 memory units, 2 clock and timing units, 2 system monitor units, 2 interrupt control units, 2 memory-to-memory transfer units, 5 CPU's, 15 channels for servicing high speed trunks, discs and printers, 160 channels for medium and low speed lines and visual display units. The units are classified as either passive (memory and matrix units) or active (rest of the units). Eight bits are used to refer to any one of the 254 units.

Every unit contains necessary data to check the validity of a data transfer or command from some other unit so that the corruption

of control or data by defective devices or programming errors can be avoided. In addition to self-checking, every inter-unit interface performs parity generation and parity checking on byte basis. Each unit is semi-autonomous. Other general features of the units useful for inter-unit transfer are:

1. control cache memory (128 bits to 512 characters),
2. ports (one or more ports),
3. maximum unit ID,
4. logical ID/Physical ID,
5. Interrupt Control Unit ID,
6. logical independence - power transient protection, malfunction detection,
7. instruction stacking of at least one instruction per port, and
8. command execution speed.

Once these general characteristics have been identified, it is easier to consider the design details of various units utilized in the CCC. Each of the individual units is described below.

A. The Matrix

The matrix unit is transparent to the user and is the functional counterpart of the bus system currently prevailing in general purpose computers. The internal structure of the matrix depends upon the following factors:

1. the total number of active and passive units implemented,
2. the number of matrix ports required for each unit,
3. the total number of memory units implemented,
4. the amount of active unit to passive unit traffic,
5. the required path availability - degree of graceful degradation, and
6. the processing load on the system.

The following assumptions are used to decide the configuration of the matrix:

1. every memory unit requires 1/2 an erlang of connection,
2. every memory unit requires two independent paths through the matrix,
3. every CPU requires .75 erlangs of connectivity,

4. every CPU requires two independent paths through the matrix,
5. channels typically require a fraction of an erlang,
6. channel-to-channel and CPU-to-CPU transfers are statistically rare,
7. discs, trunk lines, monitor units, interrupt control units, matrix control units, should be terminated with two alternate paths,
8. most other channels need not have a redundant path,
9. memory-to-memory transfers are rare (because of shared memory),
10. a distributed control, instead of a centralized control, is desirable, and
11. architectural modularity is essential and field modularity desirable.

Each functional unit is connected to the matrix via a full-duplex interface port. The CPU and memory units are each assigned 2 or 4 ports while high and low speed channels are to be provided with 2 and 1 ports, respectively. The size of the matrix greatly affects the overall speed and reliability of the system. A practical way of designing a connection matrix is to implement it in three stages. Such a scheme utilizing both time and space division is illustrated in Fig. 4.2. The matrix distributed control is based on saturation signaling. The connection to a passive unit is done through a rectangular center stage while a triangular stage routes the path to an active unit.

The following procedure is employed in establishing a connection between a source and destination unit:

1. The source unit selects a port.
2. The source unit transmits the destination identification (DID) to the matrix and the DID is propagated in parallel throughout the matrix along all encountered free links.
3. All free units receiving the DID compare it with their own logical IDs. The destination unit matching the DID, echoes back to the source.
4. The echoed DID reaches the source unit and thus a trans-

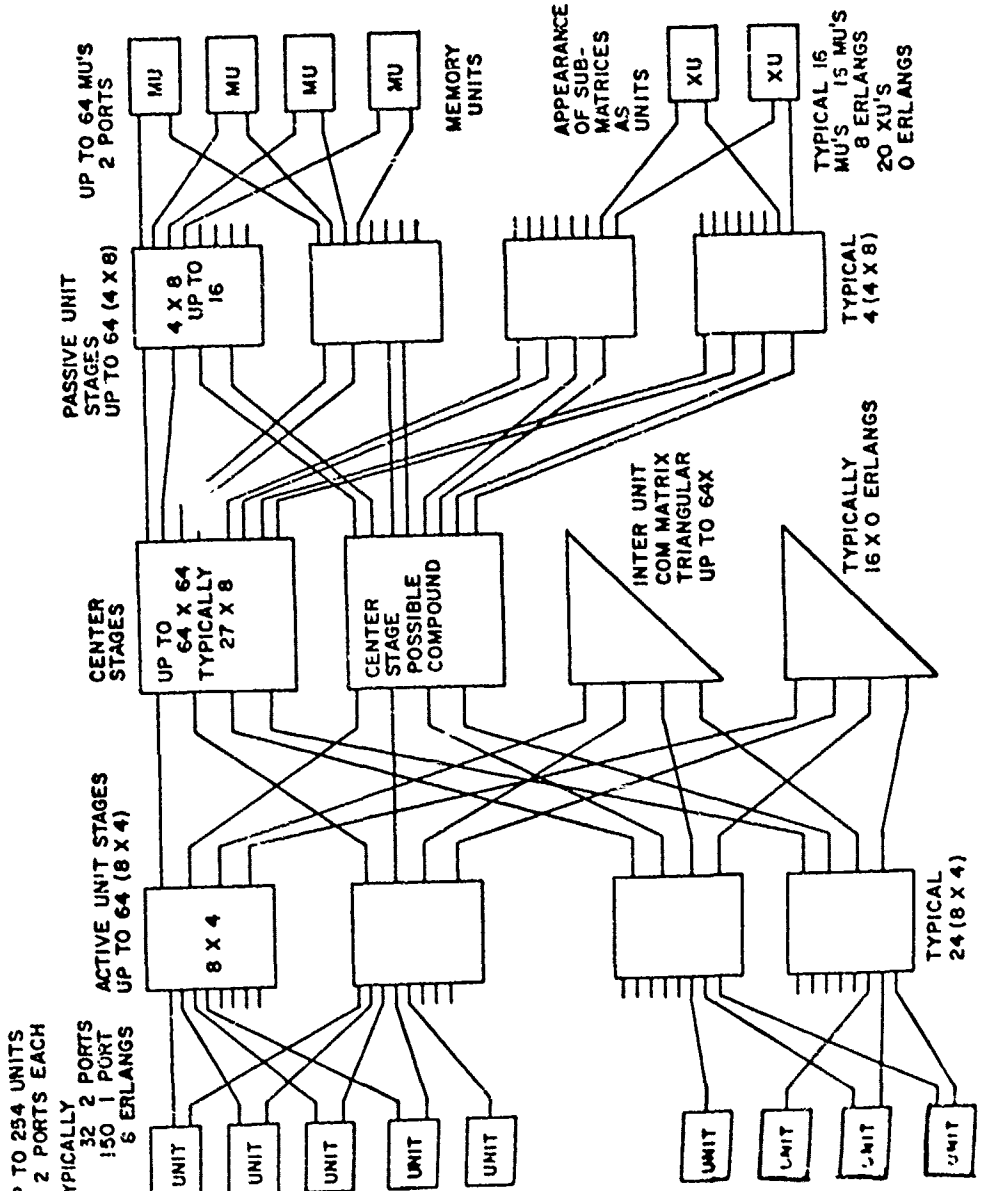


Fig. 4.2 Matrix schematic

mission path is established. All other unused links are then freed.

5. If either all possible paths are blocked or the destination unit is busy, the links remain in reserved state until paths are unblocked.
6. If the source unit receives a no-path signal, one of the following actions is taken:
   a. retry until a connection is made,
   b. try the connection via an alternate port, and
   c. try the connection with a usurpation mode.
7. The usurpation modes are used to force connections for important signals such as interrupts.
8. After establishment of the path, the source unit examines the echoed DID and compares. In case of error an interrupt is transmitted.
9. If the reflected DID matches, the source unit transmits its own ID to check for the priority structure.
10. The destination unit then changes the state of the path.
11. Then the source unit transmits a command, indicating the kind of transfer or action which is to take place.
12. If the command is valid, data is transmitted.
13. At the conclusion of the transfer, the state of the path is changed to RESERVED, holding the path for future transfers, unless usurped.

Practical implementation of the above procedure poses some design problems in the matrix and these can be identified as:

1. duplicate logical ID's,
2. blocking of return path,
3. traffic sizing,
4. matrix topology (because of pin limitations),
5. matrix timing considerations,
6. matrix depth,
7. reserve approach,
8. matrix structure (not arbitrary),
9. control signals, and
10. alternate matrix approaches.

To obtain good results, a thorough performance analysis of the matrix is needed and can be done with the aid of simulation of the matrix and other connected units. Tentatively, the following decisions are taken regarding the matrix:

a. the matrix is feasible with on-chip gate delays of 1 to 2 nanoseconds,
b. serial transfers are optimum as compared to the parallel transmission, and
c. saturation signaling is selected.

B. Memory Units

The 65,536 character memory module with 250 to 500 nanoseconds access time is addressed with a 24-bit field while 8 additional bits are utilized to indicate the logical ID (LID) number. The character organized memory allows memory-access overlapping. Each memory module contains 256 or 512 character control memory which provides the priority and the protection information associated with all other units of the CCC. The control memory layout is done in a way to accomplish maximum packing. All passive units are assigned high-order LID's. The memory protection mechanism differs from the existing practice such as:

a. it is more restrictive and structured,
b. it is associated with the memory module rather than the CPU, and
c. a similar scheme applies to all units.

C. Input/Output Operations, Channel Units and Inter Unit Repertoire

The largest part of the I/O functions are the input, the output and the storage, and I/O is extensively utilized in front-end functions, in messages switches, packet switches, concentrators and multiplexers. A good I/O structure reduces the processing load and enhances the effective use of the operating system.

The following essential characteristics are to be included in the I/O:

1. effectively unlimited number of devices,

2. unlimited number of device types (though not necessarily simulatneously),
3. maximizing the number of generic, device independent commands,
4. uniform method for handling interrupts and transfer terminations - preferably device independent,
5. minimum interference between I/O and processing,
6. isolation and encapsulation of device dependencies, and
7. minimization of I/O driver programs and subroutines - maximal commality despite device differences.

Both internal and external communications are used in CCC. Most of the internal components providing inter-unit (IU) transfers are transparent to the user. All external commands are done following a specific order of the unit, channel, device controller, and the device. The channel is characterized as:

1. channel master/slave states,
2. speed control (only in Master Mode), and
3. channel buffers (4 character buffers for each inlet and outlet).

The channel unit contains a cache memory to store a validation priority and other necessary information (via data address, data count, command chain address, data chain address, condition chain address, termination instruction) to execute the I/O transfers. The inter-unit command mode is to be distinguished as follows:

1. the identity of the unit that initiates the command,
2. the identity of the unit that receives the command,
3. the identity of the unit where the command is to be found,
4. the identities of the units that will participate in the command - that is, the units that will actually execute the command,
5. the manner in which the command will be terminated, and
6. the identity of the unit (if any) that will respond to the completion of the command.

D. The Memory-to-Memory Transfer Unit

This is used for all passive to passive units transfers by

issuing a third person command to establish connection between two passive units. The memory-to-memory transfer unit (MMTU) differs from the channels in the following characteristics:

1. fixed speed transfers (always at maximum matrix speed),
2. master master mode only,
3. no commands like HOLD, GO, HALT IN, HALT OUT, GO IN, GO OUT, HALT IN DATA, HALT OUT DATA,
4. no buffer control,
5. no dual input transfers, and
6. functionally a half-duplex rather than a full-duplex unit.

E. The Processing Unit

The processing unit is assumed to be equivalent to the CPU of a midi-computer and possesses certain unique features commonly found in large computers. Four sets of 16 registers of 32 bits length manipulable as double word, full word, half word, and byte constitute the processing unit of the CCC. The first three registers are reserved for specific functions:

Register 0: 24 bit program counter, 8 condition bits,

Register 1: 4 unit ID's - for memory unit address augmentation (i.e., page registers). The unit ID number identifies the memory unit to be accessed.

Register 2: subroutine stack pointer, 8 flag bits.

Among the four sets of registers, only one set is actively used by the Processing Unit. But this avoids the requirements of saving the contents of the register set whenever the processing state (e.g. interrupt) has to be changed and a simple switch-over from one set to another allows base level processing, high priority processing, interrupt state and all other states.

In addition, an instruction stack of 8 words is also provided for the instruction look-ahead with a possibility of instruction packing which allows storage of 7 to 32 variable-length instructions. This stack assists in executing tight loops with a minimum number of memory references. This is more effective (about 70 to 80% cases in the communication programming) whenever the relative

branch is entirely within the instruction stack.

The instruction set contains all usual arithmetic and logical operations presently available in a general purpose computer. The selection of the instruction repertoire among well-ordered and fully-packed schemes also poses an important question. In well-ordered OP-CODE, every bit has a unique and independent interpretation and is very convenient in debugging machine codes while the fully-packed system allows all possible bit combinations to be used for the instruction set. For the control unit, micro-programming technique is utilized over the hardwired control logic.

Interrupts are not handled by the processing unit. Thus, there is no need for multiple interrupt priority level in the CPU as it is taken care of by the interrupt control unit (ICU). The self-detectable interrupt condition causes the CPU to generate an interrupt signal to the ICU. The existence of malfunctions and alarm conditions that can be discovered by the CPU include:

1. power alarm,
2. parity error in received matrix transmission,
3. inter-unit micro issued by CPU rejected,
4. inter-unit micro issued by CPU not completed, and
5. interrupt chain violation.

F. The Interrupt Control Unit (ICU)

The interrupt situation is handled by any one of the two assigned ICUs. The unit transmitting interrupt to a particular CPU, is directed to the primary ICU. If the connection attempts through the matrix unit fails, it re-issues the interrupt signal to the secondary ICU. Once the interrupt message is received by the ICU, it determines what type of corrective action should be taken and on which CPU unit. The following action can be taken by the ICU:

1. forced program state change,
2. loading registers of a given set to stored values, and
3. loading of the cache memory.

Thus, the ICU is expected to perform more complicated actions. Actually, one of the CPU's is assigned to function as the ICU. The use of a CPU as a centralized ICU improves reliability because:

1. fewer unit types, and
2. more interchangeability, bigger spares pool.

It reduced the reliability as:

1. increased vulnerability of the system to a single failure as a result of centralization, and
2. the CPU/Memory combination has a higher failure rate than a special purpose ICU would probably have.

System availability and performance is improved because:

1. richer interrupt structure without compromises,
2. ability to tailor response to special situations, and
3. system wide diagnosis and ability to detect malfunctions that show up in the interaction between units.

System performance and availability is degraded because the interrupt response time is longer.

G. System Monitor Unit (SMU)

The system monitor unit acts as a "watchdog" on the CPU by initiating corrective action whenever the anticipated periodic test signals from various units of the CCC do not arrive. The SMU contains 16 to 512 characters of PROM which translates the characters as follows:

"MIN UID" - the identity of the minimum valued LID to which the SMU will respond,

"MAX UID" - the identity of the maximum valued LID to which the SMU will respond,

"SMIUD" - the logical identity of the SMU itself,

"UID X,Y,Z" - various LID to which the SMU will report should a malfunction be detected,

"T1,T2" - time period indicators, as taken from a clock signal, these are specific to the unit in the table,

"UID" - the logical ID of the unit to which the SMU will respond should a particular unit fail to report on time, and

"P" - the P fields following the MAX-UID entry are two bit port priority fields, with 00 interpreted as not allowing the specified unit to access the SMU.

The SMU also has self-testing capability.

H. System Timing and Clock Unit

The accurate time period to the CCC is supplied by the system timing and clock unit. Usually, two clock units are logically locked to each other. The control memory of the clock unit is stored in a PROM. Different fields of this PROM provides essential information like MAX and MIN UID, SELF UID, ICU-IDs, ALARM ID, priority/validation, COUNTDOWN, etc.

The clock unit can also provide the time of the day in different formats.

I. Bootstrap Unit

The automatic bootstrapping of selected unit types is done by the bootstrap unit stored in PROM and can be started by another unit through the matrix. The 65,536 characters bootstrap PROM contain first 512 characters that allows up to 256 entry points. The bootstrapping is actually a sequence of unit microcommands and properly ordered data.

J. Performance Monitor Unit

On-line hardware and software performance monitoring has now been realized to be important. The hardware monitoring is done by a set of high impedance probes that collects the data without any significant disturbance to the on-line programs. The software monitoring needs placing ter instructions at crucial points in the program. The software minotiring degree totally depends on the correct placement of the proper instructions.

K. Devices

Devices here indicate non-unit system components. These are useful in supporting the communication functions of the CCC. All devices are connected to one or more channels. The devices considered useful for the CCC are the moving head discs, the visual display units, the keyboards/printers, the digital line termination buffers, the low-speed multiple line buffers, the scanners/distributors, etc. These devices have varying capacities as well as speeds and can be selected according to the requirements of the system.

L. General Software Considerations

The software components of the CPS covers the entire computer software field. The on-line and off-line considerations and the execution probability of the modules led to the following potential software classifications useful for the CPS:

1. on-line, high execution probability software,
2. on-line, low execution probability software,
3. critical on-line software,
4. critical off-line software
5. non-critical off-line software,
6. configuration generation software,
7. system performance monitor software,
8. system analysis tools, and
9. software development tools.

The software writing can be made easier by following certain convenient rules. Various factors governing the selection of the higher level language includes universality, programmer's training requirements, simplified definition and manipulation of files, simplified creation of algorithms and processes, checking effectiveness of source syntax errors and the machine independence (i.e. transportability). Similarly, the assembler for the lower level language should include certain important features.

Testing of correct execution of each instruction in the system should be extensively done. In addition, the operational testing should be performed preferably by simulating the traffic

conditions of the system. The software development to meet the intended specifications, is of a major concern. Some of the critical areas for the software development are:

1. software development languages,
2. program modularity,
3. linking arrangements,
4. overlay,
5. executive control, and
6. overload conditions.

3. Performance Characteristics

The system architecture discussed in section 2 is simulated using a program called Generalized Analytical System Model (GASM) for message and circuit switching systems. The objective is to evaluate the performance when functions such as hardware, software and traffic characteristics are varied. The technique utilizes three different switching models for traditional message switching, packet switching and base distribution (the base distribution is a full function store and forward message switching system which provides, in addition, some circuit switching facilities as done in AMME). Furthermore, for each model, the processing task is split into a front-end function and a message switching function. Thus, in total, six models are examined. Table 4.1 indicates some of the important parameters used for the master model. Values for about 200 system parameters are assigned before the model performance is evaluated. The traffic characteristics are described in Table 4.2. The circuit switched parameters are shown in Table 4.3.

The relative weights of various features used for system evaluation are given in Table 4.4. The input rates are obtained by assuming a delay of 2, 5 and 0.2 seconds for the message switches, base switches and packet switches, respectively. These are utilized to conclude and recommand the following characteristics by observing the system performance:

1. total amount of memory,
2. number of register sets,
3. paging,

TABLE 4.1

Typical Examples of Parameters for Master Model

Description	Unit	Value
Memory and Processor Parameters:		
1. Main memory speed - for one memory cycle	μsec/cycle	1
Number of memory cycles for normal instruction (e.g., load, store)	cycles	2
2. Number of memory cycles for indexed normal instruction	cycles	2
3. Number of memory cycles for single level indirect instruction	cycles	3
4. Number of memory cycles for indexed indirect instruction	cycles	3
5. Number of memory cycles for base of long instruction (e.g., shift)	cycles	1
6. Number of memory cycles for literal mode instruction	cycles	1
7. Fraction of a memory cycle for single bit of shift	cycles	.05
8. Number of memory cycles for special instruction (e.g., extract-insert-store)	cycles	3
9. Number of memory cycles for indexed special instruction	cycles	4
10. Number of memory cycles for "short" I/O instruction	cycles	2
11. Number of memory cycles for base of indexed shifts	cycles	3
12. Number of memory cycles for program level change and return	cycles	20-30
13. Number of memory cycles for raw interrupt overhead	cycles	20-30
Network Parameters:		
1. Probability that a circuit switched line is encrypted	prob.	.8
2. Percentage of circuit switched lines that are "permanently" assigned	prob.	-
3. Total number of lines terminated at switch	number	50-400
4. Total number of Mode I lines terminated at switch	number	50-150
5. Total number of packet switched lines at switch	number	5-15
6. Average line speed	CPS	Variable
7. Number of switches connected to this one	number	6
8. Number of switches in entire network	number	20
9. Number of circuit switched trunks	number	Variable
10. Number of circuit switched trunk groups	number	10
11. Number of Routing Indicators (RI) in RI table	number	2000
12. Number of destinations in destination table	number	3000

TABLE 4.2

Traffic Characteristics of Systems

Traffic Characteristics	Packet Switch	Store and Forward Switch	Base Distribution
1. i. Number of lines per switch	40	170	380
ii. In transit storage (line blocks)	20K	60K	120K
2. Message distribution in % (Narrative/Data)	N/A	30/70%	40/60%
3. Average message length in characters (Narrative/Data)	500 (Packets)	2400	1.8K/30K
4. Multiplicity	1	2	4
5. Message processing delay Second/Message	0.06	0.85-2	2
6. Throughput:			
i. Sustained characters/second	20K	36K	95K
ii. Message arrival/second	20 (Packets)	5	1
7. Traffic by line speed:			
i. % low (up to 600 BAUD)	0%	5%	5%
ii. % medium (1200, 2400, 4800)	5%	10%	85%
iii. % high (9600)	10%	15%	10%
iv. % very high (32K)	85%	70%	0%
8. Average holding time/message:			
i. very high speed line	0.125 sec.	1-3 sec.	--
ii. high speed line	0.75 sec.	5 sec.	20 sec.
iii. medium speed line	3.5 sec.	10 sec.	65 sec.
iv. low speed line	--	100 sec.	500 sec.
9. Required % retransmission	5%	5%	5%

TABLE 4.3

Circuit Switched Systems

Parameters	Size			
No. of Lines	600	2400	4200	6000
Calls/Terminal/Busy Hour	5-8	4-7	3-6	2-5
Originated Calls/ Busy Hour	3000-4800	9600-16800	12600-25200	1200-3000
Originated Erlangs	133E-180E	360E-630E	473E-945E	450E-1125E
Loop Originated	45%	40%	35%	30%
Trunk Originated	55%	60%	65%	70%
Register Hold Time	8-12 sec	8-12 sec	8-12 sec	8-12 sec

TABLE 4.4

System Features

	Message Switch	Base Switch	Packet Switch
Message Processing Delay	2.000	5.000	0.200
Front End Delay	0.1000	0.1000	0.050
Message Processing Input Rate	2.062	1.375	1.760
Front End Input Rate	0.750	0.510	0.300
Needed Front End	2.750	2.700	5.870
Message Processing Memory	7.000	17.000	2.000
Front End Memory	2.750	2.700	5.870
Total Memory	9.750	16.700	7.870
System Weight	0.140	0.430	0.430

Average Memory = 11.93

4. number of registers,
5. indirect addressing,
6. shift instructions,
7. move instruction,
8. clear memory instruction,
9. link list instruction,
10. memory speed,
11. additional features, and
12. perifpheral memories.

4. Discussion

The proposed CCC architecture covers several important problems crucial to the CPS requirements. But there still remains some questions related to their implementation aspects and a few other considerations have not been give enough weight.

The very first thing that can be pointed out is about a more effective design of the connection matrix, which is acutally the heart of the system. The selection of a distributed connection matrix in place of a centralized unit is definitely a constructive step in designing a flexible parallel processing system. Use of cross-bar switches at each state of the network is not the only and and the best possible organization. One can easily overlook these short-comings. But the saturation-routing technique recommended for the matrix deserves a serious reconsideration. This scheme not only need a centralized control but requires a larger time delay for the establishment of a desired path. Moreover, all the free-links are kept reserved till it is possible to achieve a path between the source and the destination.

Allocation of more than one port for certain units definitely improves the performance of the system in terms of the availability by alternate path and the reliability of the system. On the other hand, this necessitates increased hardware for those units and makes the matrix design more complex. Thus, a careful consideration and allocation of ports is necessary to achieve the best possible cost-performance effectiveness. The initial connection set-up procedure takes care of a class of existing faults in the system.

But, nothing is mentioned about the reliability of the connection matrix. A thorough off-line testing and minor on-line functional checking of the matrix is essential.

In most of the existing super computers, the memory unit is usually designed to be character organized. Furthermore, every LSI based unit is designed to possess byte-wise error checking capability. Probably this might cause undue delay and it is now time to investigate the most prevalent type of faults in LSI circuits. This will not only help in reducing long-term faults but will generate guidelines to use specific hardware and software strategies for auto fault-diagnosis.

This processing unit in CCC is considered to be the CPU of a midi-computer. As advances in technology has considerably reduced the LSI chip cost, probably, is is worth exploiting the possibility of using microprocessors. If the speed is the only hesistation for their adoption, then the use of multichips, distributed arithmetic/logic unit with bit-slice microprogrammable microprocessors could be tried. The use of a centralized and simple control unit might degrade the performance of the system. A more complex ICU with well-defined interrupt hierarchy could be utilized for complex systems like CCC.

Last, but not the least, the software aspects have not been considered in enough detail. The software development cost is ever increasing and is usually a significant part of the system. The master controller for the distributed processor system has not been well-defined. The software partitioning and error recovery strategies are not properly defined.

CCC assumes all subscriber lines to be connected directly and the type of the line itself identifies the data type. In orther words, possibility of voice and data integration has been mentioned in the report. But, the functional parts processing such integrated data have never been explored. That is why the separation of different types of traffic in the integrated message has not been undertaken. As the integration of voice and date is considered to be a better way of handling the data communication, this should also be included in the overall design of the system.

CHAPTER V

GTE SYLVANIA SENET-DAX STUDY

1. Introduction

This study is aimed at enabling a high level of transmission efficiency when handling simultaneously circuit switching, packet switching and some message switched traffic. The concept of Slotted Envelope NETwork (SENET) [3] discussed in Chapter 1 has been utilized in the GTE study to design a communication processor system designated as SENET-DAX (Digital Access Exchange) scheme [16-18]. The approach is based on the use of constant period, self-synchronizing master frame to convey messages to multi-node network and each frame could be shared by a diversified class of users grouped into the following two categories:

Class I: digitized voice, low-speed video, forward error corrected facsimile, bulk 2 data from sensors, and

Class II: interactive, query/response, data base update, narrative/record, automatic repeat request facsimile, bulk 1 data and non-sensor bulk 2 data transmission and multi-access data processors.

It may be noted that the Class III users of SENET concept are treated as Class II subscribers.

The size of the two regions are allowed to vary dynamically with the instantaneous traffic conditions. To identify the beginning, each envelope starts with a header and the end of the envelope is recognized by a trailer. The optimization criteria are shown in Fig. 3.1. The Class I virtual connections require Common Channel Information Signaling (CCIS) messages and are transmitted in Class II region.

The precedence allocation and the preference protocols currently utilized in military applications can handle only limited classes of narrative/record data traffic. The SENET concept can handle simultaneously all types of voices, pseudo-voices, and data transmissions. The non-Class I data is transmitted in two different modes: A "store-and-squirt" technique for interactive query/response and the classical

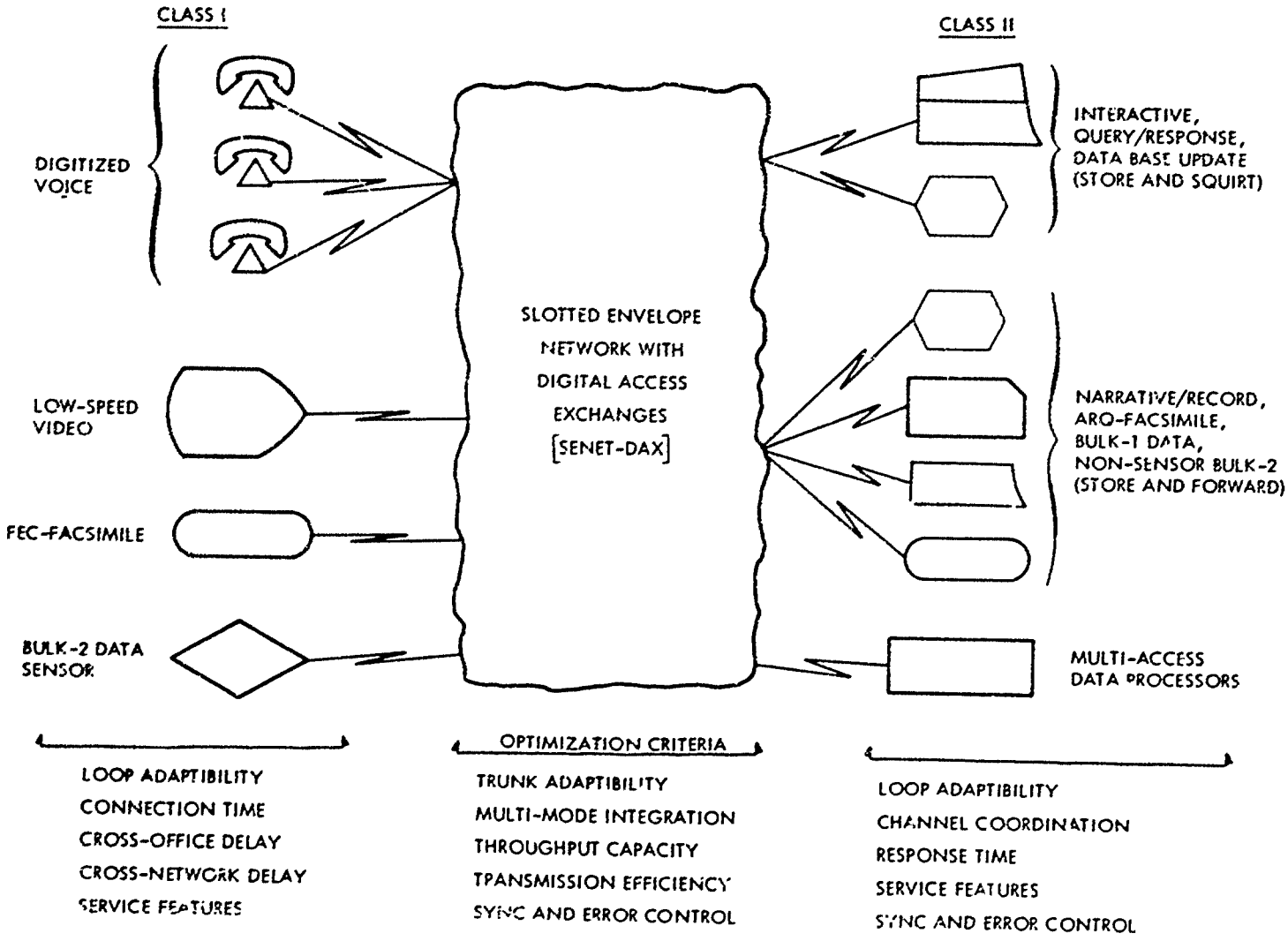


Fig. 5.1 SENET-DAX optimization criteria

"store-and-forward" technique for the narrative/record traffic. This allows more flexibility and subscriber dependent transmission strategy.

2. Architectural Description

The major considerations in SENET-DAX study are:

A. master frame structure,

B. analysis of processing requirements,

C. signaling, synchronization and error control,

D. functional allocations in the SENET-DAX system,

E. system processor architecture, and

F. equipment/software survey investigation.

A. Master Frame Structure

The structure of the master frame selected is expected to achieve the following:

1. to support subscribers using equipment characterized by digital data rates in the 8000N family, commercial common carriers, and transmission systems now under development,

2. to handle digitized voice rates representative of various evolutionary stages of development simultaneously with the data rates without mutual interferences or prohibitive inefficiency due to catering to the least efficient technique,

3. to improve the grade of service, increase the capacity, or both, as more efficient voice digitization, facsimile transmission, and video transmission digitization techniques are introduced. These improvements should be independent of each other,

4. to minimize the cross-network delays and timings involved in establishing calls, coordinating connections, crypto-synchronization, propagation of trunk signalling (CCIS) messages, error control and channel coordination in noisy or delay environments, and end-to-end control and accountibility effects, and

5. to minimize cross-office network delays and timings for implementation concepts for DAX's and integrated tandem switches.

The approach is to divide the wideband digital trunk capacities into pre-specified periods (10 msec. or 20 msec.) master frames as is shown in Fig. 5.2. The master frame starts with the Frame Marker and is shared by dynamically varying Class I and Class II Regions.

The start of Frame Marker consisting of the first N (< 100 bits) bits, is utilized for the synchronization purpose. In Class I real-time traffic, the time slice is reserved for each call and this continues during each successive frame period until redistribution of time-sharing is done because of varying traffic conditions.

The first portion of the Class II Region contains the Common Channel Information Signalling (CCIS) messages which convey information for Class I calls to be established and routed through the network. The next follows self-identifying, self-routing and of variable size Class II data packet. It also passes the information about the precedence and the security classification. Among the two approaches considered to transmit Class II messages, the Advanced Data Communication Control Procedures (ADCCP) has a better transmission efficiency and other useful features than the USASCII. The ADCCP packet normally contains the sequence of flags (8-bits), the address field (8-bits), the control field (8-bits), the information field and the frame check sequence field (16 bits). The preemption criteria for a data call (Class II) or a voice call (Class I) used is totally based on precedence value.

The dynamic assignment of Class I and Class II regions reduces the unused slice within the frame thereby reducing the inefficiency and improving the performance of the system. The Class III data of SENET concept consists of Bulk Data having the following characteristics:

1. cross-network connection time of 30 to 60 seconds,
2. variable input data rates from 100 Kb/s to 1 Mb/s,

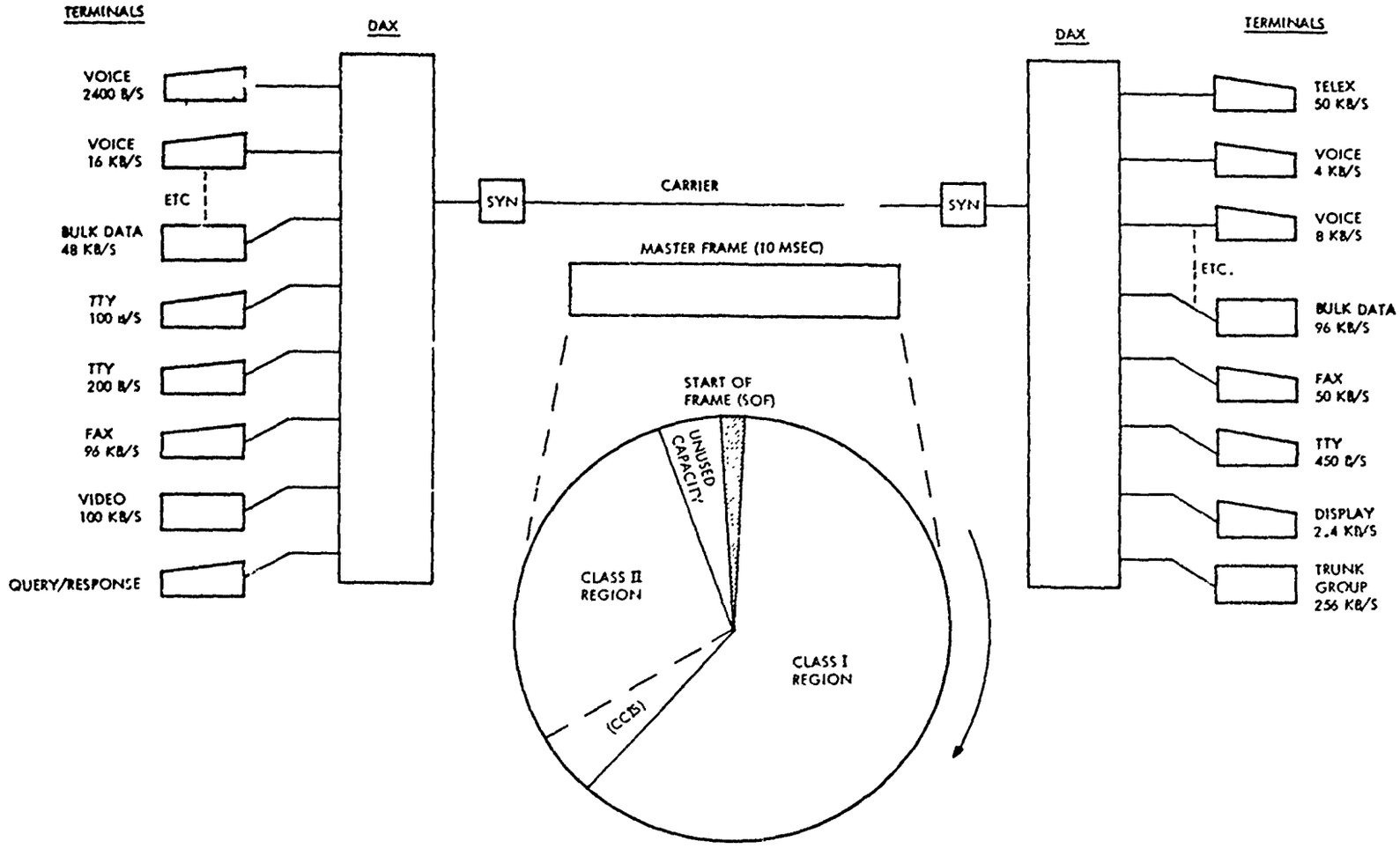


Fig. 5.2 Allocation of the master frame on a DAX link.

3. error control is required, and

4. perogative of system to terminate call temporarily.

The transfer of bulk 2 data (message length of 1 to 100 million bits) from sensor is accomplished as a Class I virtual connection while Bulk I (10,000 to 1 million bits) and non-sensor Bulk 2 transfer is achieved as a Class II packet-switched call. The error control for the bulk data transfers is achieved by segmenting data messages and providing cyclically-coded Frame Check Sequence.

The CCIS messages are short digital control messages. In addition to providing information to establish, terminate and route Class I calls through the network, the CCIS messages are also used for Class II coordination, error control, synchronization, recovery, maintenance and accountability. The changes in time slice allocation in the master frame is done only when changes are required in the Class I region. This reduces overhead due to the frequent interruption otherwise. The following CCIS messages are necessary to establish and terminate Class I calls:

1. call initiate,
2. call complete,
3. call answer,
4. release,
5. preempt release,
6. operator recall,
7. acknowledge,
8. non-acknowledge,
9. glare,
10. out-of-service,
11. all trunk busy, equipment busy, invalid route,
12. unassigned or invalid number, incompatible connection, called party unavailable,
13. call forwarding,
14. acknowledge call initiate,
15. synchronization messages,
16. CCIS keep alive,
17. maintenance,

18. traffic statistics,
19. realignment, and
20. reinitiate synchronization.

The CCIS formats and field sizes are shown in Fig. 53.

B. Analysis of Processing Requirements

The Common Channel Information Signaling (CCIS) messages used to control the individual subscriber channels, are expected to satisfy the following:

1. permit processor software determination of varying Class I/Class II boundary on a frame-by-frame basis,
2. permit dynamic remapping of the switched data channels in the Class I region on a DAX-to-DAX interactive basis,
3. provide for the establishment and breakdown of switched data calls of routine precedence,
4. provide for handling of pre-emptive switched data calls,
5. provide for DAX-to-DAX transfer of administrative traffic, e.g. automatic message accounting (AMA) data, SYSCON messages, etc.
6. minimize cross-network time from dialing of the last digit by the subscriber to provision of ringback to the subscriber, and
7. maximize utilization of Class I region; i.e. allocation of channels no larger and no earlier than necessary, dropping of channels as soon as possible after release of call(s), repacking of Class I region as soon as channel(s) are dropped.

Among the two approaches, (i.e. the Originating Office Control and the Spill Forward Control) for the CCIS directed call signaling and routing, the use of the second approach with a suitable moderation is recommended. In this modified method, any switch spills over signal only to an adjacent switch and in the case of blocking in the primary link, the switch forwards the call via alternate links. Four different strategies for the Class I Region Channel Allocation are also considered and the steps for establishing and breaking down Class I calls are also

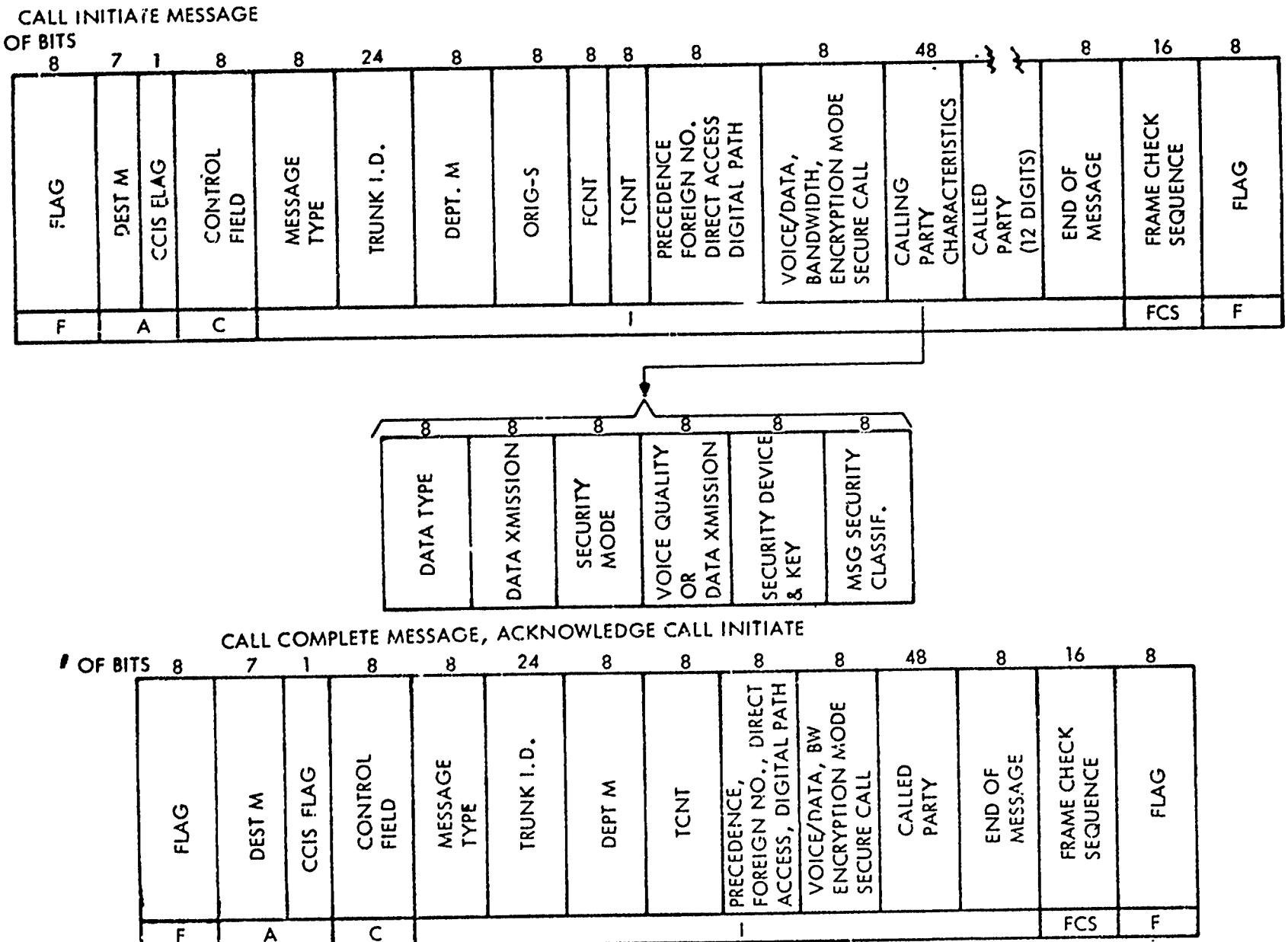


Fig. 5.3 CCIS formats and field sizes

covered in detail. If pre-empting of call(s) is/are essential, then it is done in reverse precedence order while the security violation is also properly taken care of.

The Class II data packets self-contain the necessary link and the network control information and the adaptive routing of Class II traffic is done similar to the Class I traffic but on a per-packet basis. In the situation where there is insufficient room, a smaller packet of a lower precedence is transmitted.

The accountability of traffic due to dynamic alternate routing and recovery from interruptions (both transient and catastrophic) has also been considered. For Class I traffic, it includes:

1. overall call accountability,
2. CCIS message accountability,
3. routing accountability,
4. channel accountability,
5. precedence accountability,
6. security accountability, and
7. trunk group accountability.

The Class II traffic accountability includes:

1. overall call accountability,
2. message accountability,
3. packet accountability, and
4. precedence and security accountability.

A high degree of the system availability and maintainability is achieved by continuous hardware and both on-line and off-line software and a synchronized standby duplicate unit is constantly available while the failed unit is being tested. The major phases of the maintenance philosophy is given in the Table 5.1.

C. Signaling, Synchronization and Error Control

The DAX services are provided to the following three general categories:

1. telephone instruments - transmitting at various data rates (2400 b/s to 50 kb/s) and employing either digital or analog signaling and supervision.
2. data terminals - transmitting at various data rates

TABLE 5.1

Maintenance Methodology

1. Establishment of a Failure Occurance
   a. Detection of the Failure
   b. Verification that a Failure has occurred
   c. Classification of the Failure as Catastrophic or Transient
   d. Fault Localization to a Point or Points in the Network and Communication to Central Node
   e. Indication of Points in the Network where Fault had an Impact
2. Reconfiguration to Restore Full Operation
   a. Disabling the Unit in which the Existence of a Failure has been Established
   b. Removal of Failed Unit
   c. Replacement with a Spare Unit (or Switchover)
   d. Initialization of Replacement
   e. Resumption of Normal Operation
3. Repair of the Failed Element
   a. Localization of Failure indications
   b. Isolation of a Unit which is Replaceable
   c. Replacement and Power-Up
   d. Initialization Checkout
   e. Restoration and/or Recovery
   f. Enablement of Switch-In (if applicable)

(75 b/s to 200 kb/s), using either character or message formats, various procedures, and operating either synchronously or asynchronously by character or message, and

3. computers - transmitting at various data rates (4800 b/s and above), using either message or packet formats, various procedures and operating asynchronously by message or packet.

The three phases of a DAX subscriber are the call initiation, the data transfer and the call termination. Class I terminals consist of the telephone instrument or data terminal requiring circuit switched service. Class II terminals contain the message and packet procedural equipment including teletype, facsimile, paper tape, computers, etc. Seven modes of operations are provided for Class II subscribers. Six of them are message oriented as used in AUTODIN and the seventh is to be used by packet terminals.

Two types of interface, one for voice subscribers (telephone), and the other for the data subscribers (terminals and computers) are also suggested. The Frame Synchronization is essential to minimize the transmission overhead, to realize a cost effective hardware implementation and to reduce the burden on the DAX processor(s). A special hardware called Frame Maintenance Unit, is assigned to each full-duplex inter-DAX link for the synchronization monitoring. For data terminals, a Line Interface Unit is provided for bit-synchronization.

The format change at both the originating and terminating nodes for Class I virtual circuit switched data creates a little problem. The loss of bit integrity due to dynamic assignment of channels is avoided by buffering all data at each node. But such a delay is not necessary for the Class II pseudo real time packet switched services.

To ascertain satisfactory transmission/receiving of data in DAX network via connected nodes, it is essential to incorporate internode and intranode synchronization. The first includes bit synchronization (network bit integrity) and master frame synchronization on a link-by-link basis. The second concerns master

frame alignment and coordination at each node. Various synchronization schemes are evaluated in the light of factors like survivability, cost, reliability, complexity, etc. The disturbances caused by the transmission delay variations in links like the coaxial cable and the microwave radio are also considered.

The inherent self-checking characteristics of ADCCP packets utilized in CCIS messages allows error control of the following DAX network parameters: type and average transmission rate of CCIS messages; noise environment; and retransmission scheme. The ADCCP error handling capacity is augmented with the use of Forward Error Correction (FEC). The three basic techniques for error control in a data network are:

1. error detection and retransmission of the data found to contain errors (usually referred to as Automatic Repeat Request),
2. FEC (errors remaining after the correction phase are passed on along with the good data), and
3. FEC followed by error detection and retransmission.

D. Functional Allocations in the SENET-DAX System

The subscriber requirements can be summarized as follows:

1. short transmission time, systematically or occasionally,
2. simplex, conversational, or inquiry/response-type communications,
3. transmission of large volumes of data,
4. temporary storage of data received outside office hours and automatic retransmission at office opening time,
5. automatic transfer of incoming traffic to an alternative terminal,
6. possibility of carrying out some simple processing in the switching centers,
7. low error rate,
8. security of transmission,
9. mode/code/speed/format conversions, and
10. data operation facilities.

The subscriber-related service features voice/data equivalence

for both Class I and Class II are listed in Table 5.2.

The impact of subscriber features on the network include the capacity, speed and cost of the network as affected by the individual service of interest. The major measures of network performance are:

1. traffic throughput,
2. network grade of service,
3. link grade of service,
4. call completion and data transfer speed,
5. network control complexity, and
6. special equipment.

The impact of Class I and Class II and the system service features on the network are also outlined.

E. System Processor Architecture

The compatibility of various architectures have been examined according to the stringent requirement of the SENET-DAX concept. A higher level of diagnostic capabilities are essential since reliability is of paramount concern. Both existing and proposed uni-processor and multi-processor architectures have been considered. A single processor is seen to be unable to provide software servicing required for the SENET-DAX system. The multiprocessor/multimemory interconnect structure designed by the Carnegie-Mellon University exhibits modular growth in terms of trunk and access servicing. The main shortcoming in this system is the amount of reliability provided by the system. The redundancy of several single thread elements have an impact on the cost and complexity. Methodologies for task allocation for pipeline processing are not clear and the complex system software for the processors control produces a negative effect on the performance.

The multiple processing system again poses an interesting question of having a shared memory or private memories. With the shared memory system, the multiprogramming approach for performance enhancement is excessively degraded by the memory access conflicts. Thus, neither shared memory system nor a high

TABLE 5.2

SENET-DAX Subscriber Service Features

Class I	Class II
Precedence and Preemption	Precedence and Preemption
Conferencing	Multiple Addressing
Intercept	Intercept
Data Service	Universal Data Subscriber Interface
Secure Mode Conversion	Mode/Code/Speed/Format Conversion Message/Communications Line Security
Compressed/Abbreviated Dialing	(No Equivalent)
Call Transfer/Forwarding	(No Equivalent)
Automatic Group Hunting	(No Equivalent)
Attendant/Operator Functions	(No Equivalent)
Direct Access Service	(No Equivalent)
(No Equivalent)	Message Accountability
(No Equivalent)	Archival Storage
(No Equivalent)	Retrieval and Trace

level of multiprogramming is suitable as compared to the distributed memory system.

In the distributed system architecture the data throughput rate is increased by the multiple processor/memory interconnect system while graceful single failure degradation and distributed diagnostic capabilities are still provided. Probably the inter-processor communications overhead can be large.

The functional block diagram of the SENET-DAX model distributed architecture is shown in Fig. 5.4. All nodal activities are performed via a two level fully bi-directional bus and three hardware/software groups (i.e. the nodel equipment group, the trunk line group and the local access group) are attached to this bus. The nodal processor performs minimal supervisory control over nodal activities. The bus with six ports can service one local access group and a maximum of five trunk line hardware/software groups, each servicing one full-duplex trunk line at a maximum rate of 230.4 kb/s. The local access port is interfaced to a maximum of eleven Class I and at least one Class II subscribers via their respective processors.

The recommanded functional architecture is shown in Fig. 5.5. All processors have an attached program memory. The control FIFO's receive all bus transfer related control information. At the link bus port, the link output processor takes care of the prepared packet.

The software allocations can be divided into the functions expected from the link port, access port, and nodal processors.

1. The Link Port Processor Functions are:
    a. Input Processor
        i. initialization and initial Class II link list allocation (Data),
        ii. CCIS analysis and generation,
        iii. routing,
        iv. control switching,
        v. list management (input map, deck, sequence number, free list),
        vi. test/disgnostic, and

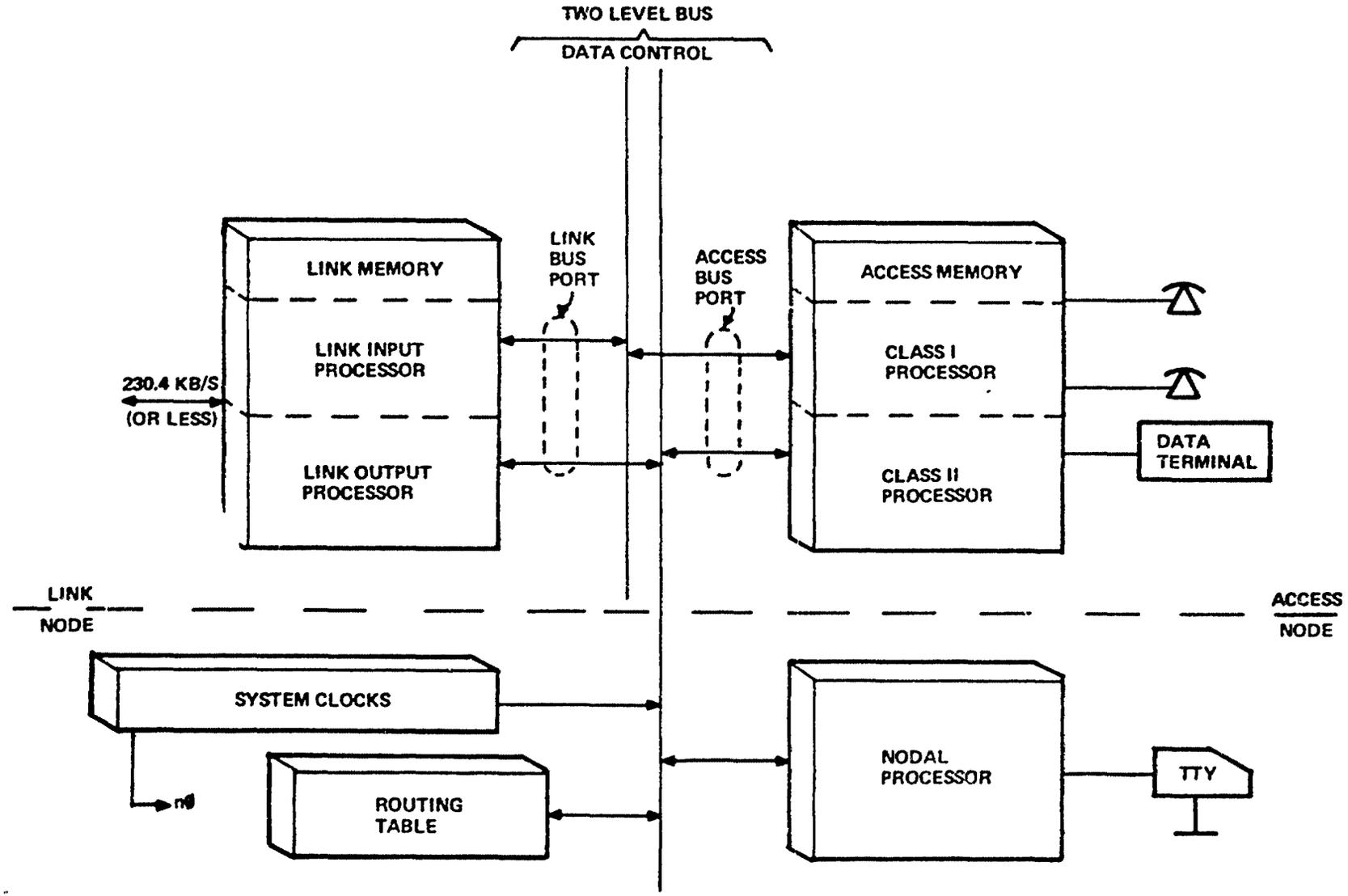


Fig. 5.4 SENET-DAX functional block diagram

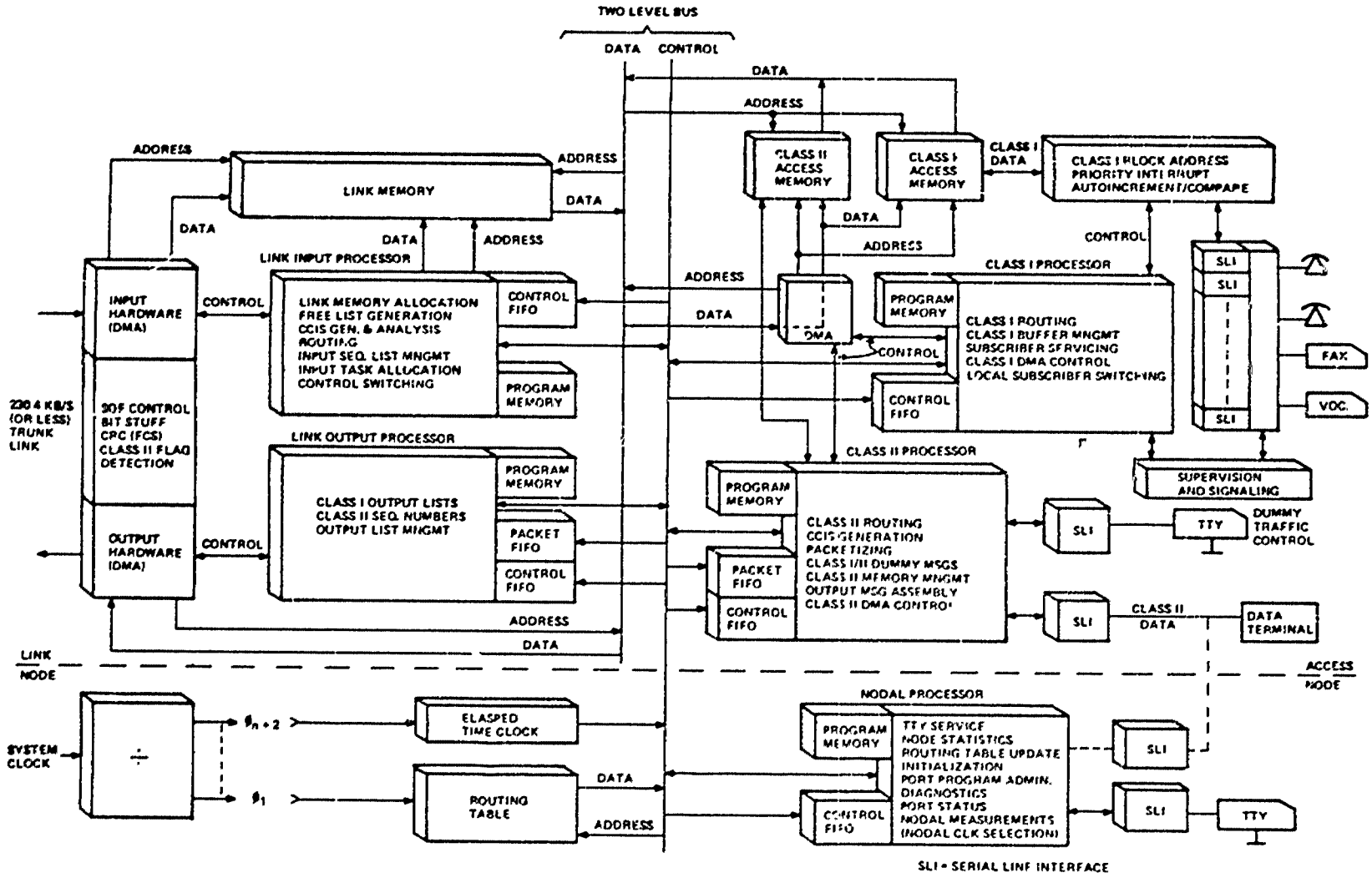


Fig. 5.5 SENET-DAX functional architecture

vii. statistics.

b. Output processor

i. initialization and Class II link list allocation (program),

ii. Class 1 list processing (program),

iii. Class II list and queue processing (program),

iv. test/d'agnostic, and

v. statistics.

These processors operate in a background/foreground mode and the interrupt service routine services real-time line control interface requests.

2. Nodal Processor Functions are:

(a) I/O control function (TTY),

(b) initialization,

(c) link and node administration,

(d) routing/traffic updates,

(e) test/diagnostic - link status,

(f) node statistics/measurements, and

(g) debugging aids.

3. Access Port Processor Functions include the servicing of continuous and rapid digital bit stream and this requires functional separation of Class 1 and Class II data. One processor takes care of only one class of traffic. The detailed functions to be performed are:

a. Class I Processor:

i. Class I buffer management - classmark processing and subscriber buffer allocation based on 10 msec,

ii. routing - outgoing link selection via routing table,

iii. Class I DMA control - Class 1 buffer address transfers by DMA from various port data memories,

iv. local subscriber supervision/signaling scan and control, and

v. local subscriber switching - address manipulation of Class I memory to create a cross-connected bi-directional data flow.

b. Class II Processor:

i. Class II buffer management - similar to Class I, 30 word blocks is managed as a free list memory resource for dynamically processing generated outgoing packets.

ii. routing - outgoing link selection resulting from internal processing and buffer address transfer,

iii. CCIS generation/analysis - outgoing "call initiate" message types and initiation of Class I processes for received packets.

iv. packetizing and depacketizing - may be combined with message assembly function for device specific buffers based on terminal rate; packetizing routines will utilize Class II access memory free list buffers for packet generation.

v. Class II DMA control - Class II buffer address transfers by DMA from various port data memories, and

vi. Class I/II "Dummy" message header generation/control - generation of table-driven Class I and Class II simulated traffic by console request processing.

The selection of the design for SENET-DAX is based on the design considerations, timing analysis and hardware design for cost estimates.

F. Equipment/Software Survey Investigation

The microprocessors and LSI circuits have created a revolution in all possible areas of general interest. The selection of a specific micro for a specific application is more complex and it needs more careful investigation. Presently, 4, 8, 12, and 16-bit

processors are commercially available. The continuous advancements in bipolar technology has yielded 2o bit-slice microprocessor chips that makes the design of an arithmetic/logic unit and I/O interfaces modular and can be microprogrammed according to the requirements. All these LSI devices are highly reliable and require very low power as compared to large computers.

In order to evaluate a specific microcomputer family, one has to consider the following characteristics:

1. software characteristics,
2. macro assembly language,
3. system implementation languages,
4. operational capability, availability and cost, and
5. development system off-line.

The integrated system concept has been examined in a four-node experimental network configuration.

3. Performance Characteristics

To evaluate the performance of the proposed system, certain parameter values are assigned. Assuming the maximum traffic of 500 packets/second with an average figure of 200 and 13 calls/100 seconds. The real-time clock interrupt of 1 ms and the average processor execution time is taken as 3 microseconds/instruction. These figures lead to the input and output link processor timings as is given in Table 5.3. The variation of transmission efficiency, throughput and optimized packet size is calculated for varying values of bit error rate for block-by-block ARQ (Automatic Repeat Request) and is shown in Table 5.4.

For the packet size of 224 bits, the variation of the link data capacity as a function of the voice traffic load is shown in Table 5.5. The blocking probability of voice calls and expected delay for data messages are important factors reflecting the performance of the system. Their variation for two different transmission rates are shown in Table 5.6 and 5.7.

A single 230.4 kb/s link in the proposed scheme is said to be able to support up to 20 voice subscribers and 360 data subscribers. In arriving at these values, the following voice traffic is assumed:

1. an average holding time of 3 minutes for local calls and

TABLE 5.3

Link Input and Output Processors Timing Summary

	Loading at the rate of 500 packets/sec		Loading at the rate of 200 packets/sec	
	Input Processor	Output Processor	Input Processor	Output Processor
Real-Time Clock Routine	16.0%	16.0%	16/0%	16.0%
Control Schedular	7.8%	7.8%	7.8%	7.8%
Free Memory-List Management	2.2%	2.2%	0.9%	0.9%
Packet Analysis	30.0%		12.0%	
Translation	4.5%		1.8%	
Routing	4.2%		1.7%	
CCIS Packet Generation	0.03%		0.03%	
Transmit Packet Control	6.0%		2.4%	
Acknowledge/No Acknowledge	7.5%		3.0%	
Background Queue Processing		12.0%		4.8%
Timeout Processing		0.1%		0.1%
Output Address Generator		9.0%		3.6%
Maintenance Statistics	0.6%	0.6%	0.6%	0.6%
Total Processor Loading	78.8%	47.7%	46.2%	33.8%
Reserve	21.2%	25.0%	25.0%	25.0%

TABLE 5.4

Optimization of Transmission Efficiency and Throughput for Different ARQ Protocols

ARQ Protocol	Bit Error Rate	Optimum Packet Size (Bits)	Optimum Transmission Efficiency	Optimum Throughput (KBPS)	Packet Error Rate
Block-by-Block	10^{-3}	728	.1617	7.24	.5111
	10^{-4}	3,109	.4840	21.68	.2672
	10^{-5}	10,977	.7583	33.97	.1040
	10^{-6}	35,953	.8836	39.59	.0353
	10^{-7}	115,025	.9284	41.59	.0114
Continuous Type I	10^{-3}	313	.2744	12.29	.2614
	10^{-4}	827	.7226	32.37	.0794
	10^{-5}	85	.8930	40.01	.0245
	10^{-6}	.785	.9342	41.85	.0078
	10^{-7}	24,360	.9452	42.34	.0024
Continuous Type II (only erroneous packet repeated)	10^{-3}	224	.467	20.92	.2007
	10^{-4}	600	.763	34.18	.0582
	10^{-5}	1,798	.8869	39.73	.0178
	10^{-6}	5,586	.9296	41.65	.0056
	10^{-7}	17,566	.9435	42.27	.0018

TABLE 5.5

Data Utilization as a Function of Offered Voice Traffic

Busy Hour Data Load (2 Packets)	Offered Voice Traffic (Erlangs)	Percent of Frame Available for Data (Error Free)	Percent of Frame Available for Data (Taling into Account Channel Errors)	Data Utilization Factor	Total Trunk Utilization
19.44%	0	88.80%	41.48%	46.87%	52.86%
"	1	82.07	38.33	50.72	59.59
"	2	75.35	35.18	55.26	66.32
"	3	68.62	32.05	60.66	73.05
"	4	61.89	28.90	67.28	79.77
"	5	55.16	25.76	75.47	86.50
"	6	48.44	22.62	85.94	93.23
"	7	41.71	19.47	99.84	99.74
"	8	34.98	16.33	Overload	Overload

TABLE 5.6

Variation of the Waiting Time and Data Utilization with Offered Data Traffic for Fixed and Movable Boundary Cases; 230.4 KBPS Transmission Rate

Data Packets Offered	Prol. of Blocking (4 Erlangs) (Voice)	Voice Utilization	Fixed Boundary		Movable Boundary		Total Trunk Utilization
			Waiting Time (msec)	Data Utilization	Waiting Time (msec)	Data Utilization	
1	.1%	0.34	∞	-	15.0012	.158	.478
2	.1%	0.34	∞	-	15.045	.316	.576
3	.1%	0.34	∞	-	15.33	.473	.673
4	.1%	0.34	∞	-	16.87	.631	.770
5	.1%	0.34	∞	-	20.81	.789	.867
6	.1%	0.34	∞	-	∞	-	-
7	-	-	∞	-	∞	-	-

TABLE 3.7

Variation of the Waiting Time and Data Utilization with Offered Data Traffic for Fixed and Movable Boundary Cases; T1 Carrier Rate

Data Packets Offered	Prob. of Blocking (63.5 Erlangs Voice)	Voice Utilization	Fixed Boundary		Movable Boundary		Total Trunk Utilization
			Waiting Time (msec)	Data Utilization	Waiting Time (msec)	Data Utilization	
1	.1%	.89858	15.0093	.178	15.0000	.042	.671
2	.1%	.89858	15.1900	.359	15.0000	.085	.686
3	.1%	.89858	16.1803	.534	15.0000	.127	.700
4	.1%	.89858	20.5555	.713	15.0000	.169	.715
5	.1%	.89858	∞	-	15.0000	.212	.729
6	.1%	.89858	∞	-	15.0000	.254	.744
7	.1%	.89858	∞	-	15.0000	.296	.758
10	.1%	.89858	∞	-	15.0002	.424	.802
15	.1%	.89858	∞	-	15.0475	.635	.874
20	.1%	.89858	∞	-	16.2050	.847	.947
23	.1%	.89858	∞	-	∞	-	-
25	-	-	∞	-	∞	-	-

5 minutes for trunk calls,

2. a call distribution by transmission rate given by:
   10% at 2400 bits/sec,
   10% at 4000 bits/sec,
   15% at 8000 bits/sec,
   50% at 16,000 bits/sec,
   10% at 32,000 bits/sec,
   5% at 50,000 bits/sec, and
3. all calls are full-duplex.

4. Discussion

In the proposed nodal processor system, a two level bus structure is utilized and the memory contention problem can be avoided only by an efficient connection network. A single link with the master processor of the node is not at all sufficient. Similarily, inter-node communication line alternate paths introduces redundancy in the system and causes increased implementation cost, it does provide improved availability and reliability of the system.

The two-memory system nodal processor also suffers from the conflict problem and there is a need for larger number of small memory modules. The graceful degradation capability should also be considered. In the system, only one port is allocated to the trunk lines. Such a dedicated assignment is definitely efficient if we assume that the amount of trunk traffic is expected to be substantially greater than the local use. This might be true on the average basis. But the same ratio may not hold good for the instantaneous traffic conditions. A thorough investigation of the expected traffic situations is essential. It is believed that a better overall throughput of the system can be achieved by optimizing the sharing of the resources and the dynamically varying port allocations might be helpful in this respect.

With ever-increasing costs of software, much emphasis should be directed towards specifying modular operating systems. The adopted language should be carefully evaluated in the light of important factors like portability, universality, etc. It is worth investigating the use of roving master processor at each node. This makes testing of the master-processor possible and the roving master technique avoids the system failure because of only one faulty processor. Moreover, on-line and off-line error diagnostic strategies need to be clearly defined.

CHAPTER VI

CARNEGIE-MELLON C.mmp AND Cm*

1. Introduction

The Carnegie-Mellon University multi-mini-processor C.mmp was designed to satisfy the computation requirements of research projects and to investigate the computer structure [20]. The main constituents of C.mmp are shown in Fig. 4.1. It consists of up to 16 miniprocessors (DEC PDP-11/20 and PDP-11/40) and a large shared memory with a possible interconnection between a processor and the memory via the cross-bar switches denoted by S_{mp}. The processor and manually controlled switches S_{kp} enable a link between each processor and controllers (K_{io}) which in turn allow access to the secondary memories and I/O devices.

A small local primary memory M_p associated with each computer reduces the band-width requirements and allows it to function as a completely independent computer and to take care of off-line maintenance. But the local memory is not available for the user. The data operations component, D_{map}, transforms the processor-furnished address to a physical memory address. This way 16 processors P_c can concurrently communicate with all of the 16 shared memory ports M_s. The problem comes only when more than one processor wants to have an access to memory locations in the same port serving up to 65 K-bit words. An effort to resolve the contention is done by obtaining the statistical distribution of memory references and taking hardware and software measures such as proper page placement and utilization of cache for co-ordination between the processors.

The operating system of C.mmp consists of a "kernel" and "multi-layered standard extensions." The kernel provides only bare essential tools for the operating system and includes only the creation of a virtual machine to support user programs and functions of a resource manager and allocator. The kernel part can back up a number of extensions which take care of other mechanisms of the operating system.

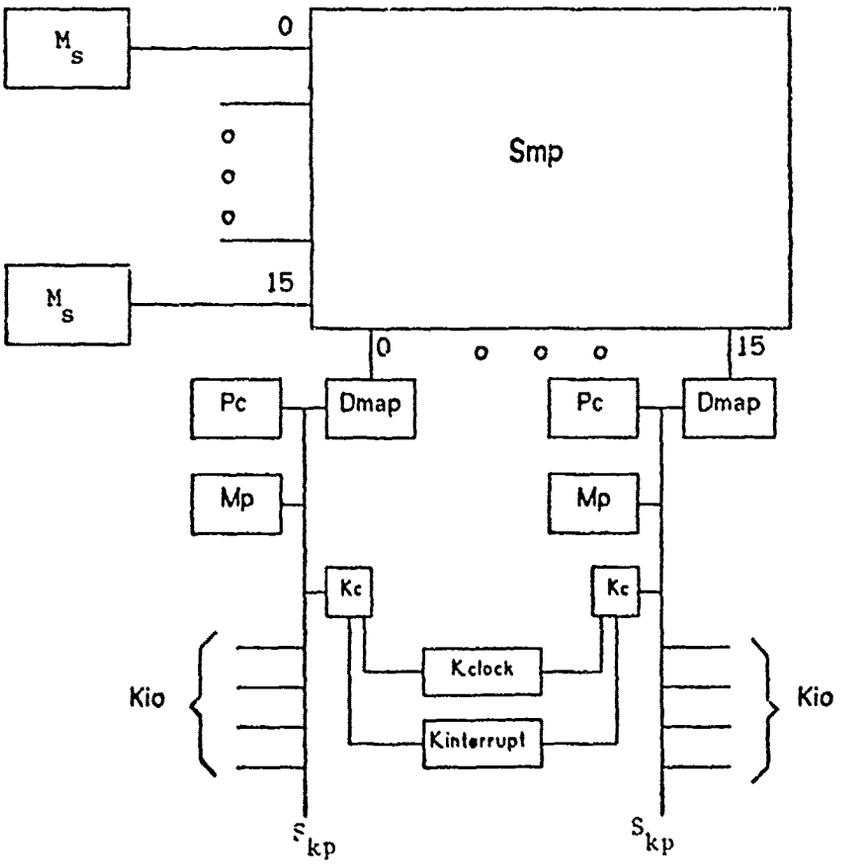

Ms
0
Smp
Ms
15
0
15
Pc
Dmap
Pc
Dmap
Mp
Mp
Kc
Kc
Kclock
Kinterrupt
Kio
Kio
Skp
Skp

Fig. 6.1 C.mmp

To make the system more reliable, multiple copies of critical data are stored and important results are obtained by comparing the results of two distinct methods computed on the same or on two different processors. The hardware functioning is tested at fixed intervals or applying the diagnostic test when the processor is idle.

The descendant of C.mmp is Cm* which stands for an arbitrary number of multi-microprocessor computer systems and is shown in Fig. 6.2. Most of the basic ideas and the architectural features contained in C.mmp are followed in Cm*. The processor-memory module is called computer module of C_M. A low concurrency network of buses give access to shared memory. The local memory to a processor is also shared.

The S_{local} provides the first level of memory mapping to the processor's local memory while outside access requests are made via the K_{map}. All non-local memory references are performed by message switching with each message buffered until the receipt of a positive answer. The memory request outside the cluster of C_Ms and a K_{map} is done through intercluster buses.

2. Description

A. Utilized Communication Concept

The possibility of using C.mmp for the communication network has been explored by emulating the behavior of a single node in an integrated circuit-packet-switching communication network [19,28]. The transmission integration is based on the SENET scheme which requires classification of traffics into three categories: Class I, Class II and Class III. The details of the modified frame are shown in Fig. 6.3. It starts from a certain number of bits for Common Channel Information Signalling (CCIS). Then follows a Class I region. The rest of the frame is occupied by the Class II which also includes Class III data and hence no distinction is made between the two classes of traffic. Class I data is transmitted in fixed slots, one allocated for each logical channel currently in use. Thus Class I data is either accepted or rejected, with short connection delays and without error control. Class II traffic is always accepted but may incur a system delay with short connection and cross-network delays. The Class II data is transmitted as disjoint packets and requires a high degree of reliability.

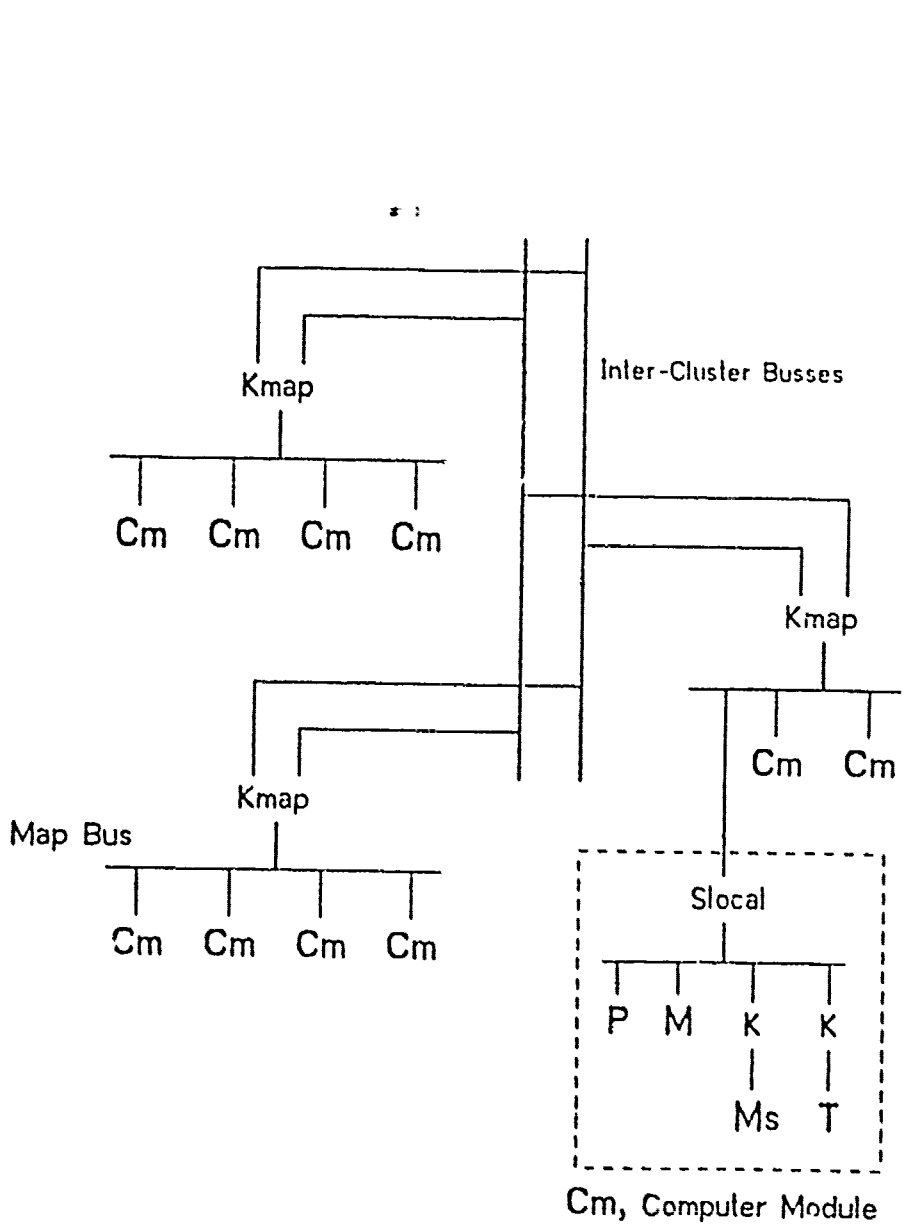

Inter-Cluster Busses
Kmap
Cm Cm Cm Cm
Kmap
Cm Cm
Kmap
Map Bus
Cm Cm Cm Cm
Slocal
P M K K
Ms T
Cm, Computer Module

Fig. 6.2 Cm*

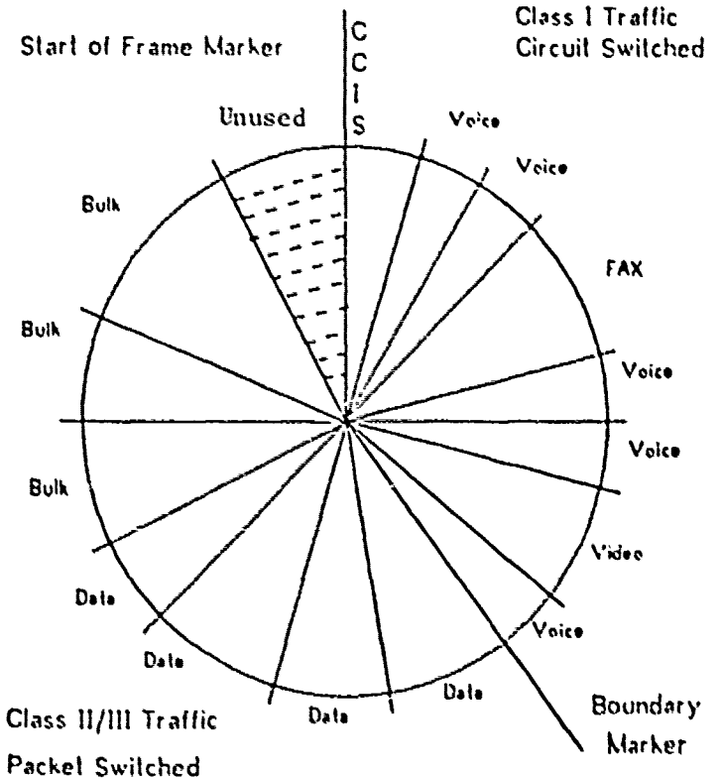


Fig. 6.3 An integrated network frame

To fulfill the real time requirements of Class I traffic, Routing Tables internal to the integrated switches are utilized that reflect the establishment of a logical circuit on each switch along the two subscribers. The entries reservation in the routing tables is done during the initial set-up and remains unchanged until the termination of the communication. These tables also contain information about the slot type (Voice, Video, etc.) and precedence. The non-homogeneous links and asynchronous behavior of links do not pose any problem as the time-allocation for each frame is kept fixed while the length is allowed to vary according to the capacity of the link.

The link functions are performed by special purpose hardware called Line Interface Device (LID). The packet transmission format utilizes hardware-generated header and trailer fields. The trailer field would contain the cyclic redundancy field for Class II packets and the flag-character to indicate the end of the packet. A Channel Command Vector (CCV) is created in the switch processor's memory indicating the count and starting address of various packets to be transmitted in each frame. The Common Channel Information Signalling (CCIS) field used to transfer Class I routing tables, itself is not transmitted as Class I packet. But to include error-checking capability, it is processed as Class II data packet.

B. Task Decomposition

On C.mmp, a cluster of processors sharing both code and storage is used to emulate a single integrated witch. Other processors, external to the cluster are used to simulate the network and are responsible for feeding multiple frame streams (simulating multiple, asynchronous, input channels) and collecting statistics about the behaviour of the integrated switch. Both inter- and intra-cluster ommunication and synchronization are implemented by sharing buffers and interlocks accessable by the individual processors.

The functional decomposition of the integrated switches leads to two categories: the relay and the regional functions. Relay functions include those to be performed to establish and maintain communication with the other switches and regional functions includes those needed to establish and maintain the accessability to the network by the local subscribers. These functions are given below:

1. Relay Functions (Trunk lines)
   a. Routing selection
      i. choice of output line to send message out on, including messages originating at this node,
      ii. essentialiy table-driven at this level.
   b. Message acknowledgement
      i. acknowledging received messages,
      ii. timeout on expected acknowledgements for sent messages.
   c. Channel discipline
      i. frame decomposition and assembly,
      ii. allocating/compacting real-time message slots in frames.
   *d. Maintenance of routing tables
      i. timing of message delays to neighboring nodes for adaptive routing..
   **e. Hardware/software fault detection
      i. Intra-node detection: timeout, NXM, data structure integrity check, reliability analysis,
      ii. inter-node detection/correction: status of other nodes as viewed over interconnection links, external load/restart capabilities.
2. Regional Functions (Access lines)
   a. Analysis/validation/generation of packet header fields
      i. precedence check: is this terminal authorized to use this level of precedence?
      ii. security authorization check: is this terminal authorized to send/receive messages of this security level?
      iii. comparison of header security keys: do they match?
      iv. segment count: check for any missing or out-of-sequence and appropriate actions if so.
      v. generation of any necessary header information for originating messages.

b. Flow control functions:

i. access denial: refusing origination traffic for categories not being accepted by destination (e.g., because of congestion),

ii. queue-length monitoring, to detect congestion,

iii. purging of low category/precedence traffic from queues if necessary,

iv. delay of acknowledgements if congested.

c. Logical channel control:

opening/closing of logical channels, especially for real-time connections.

d. Precedence handling functions:

for high precendence messages.

*e. Identification/validation of terminals:

table lookup, possible password check, etc.

*f. Compatibility conversions:

character translation, mode/format conversions.

*g. Maintenance of regional tables:

line tables, terminal ID tables, logical channel tables, etc.

*h. Hardware/softward fault detection.

*i. Statistics gathering/reporting.

Functions marked with an asterick (*) are "outer-loop" functions, i.e. functions which require negligible execution time compared to the "inner-loop" functions.

C. Software Organization

The system is implemented as a set of procedures by using homogeneous processors and shared memory. The scheduling of the tasks is performed via a set of priority ordered queues as is shown in Fig. 6.4.

A significant amount of redundancy carried in Class I traffic allows tolerance of a larger error and hence error-checking and generating acknowledgments for Class I packets can be avoided. But the establishment and maintenance of a Class I channel is critical and the control messages are transmitted as Class II packets.

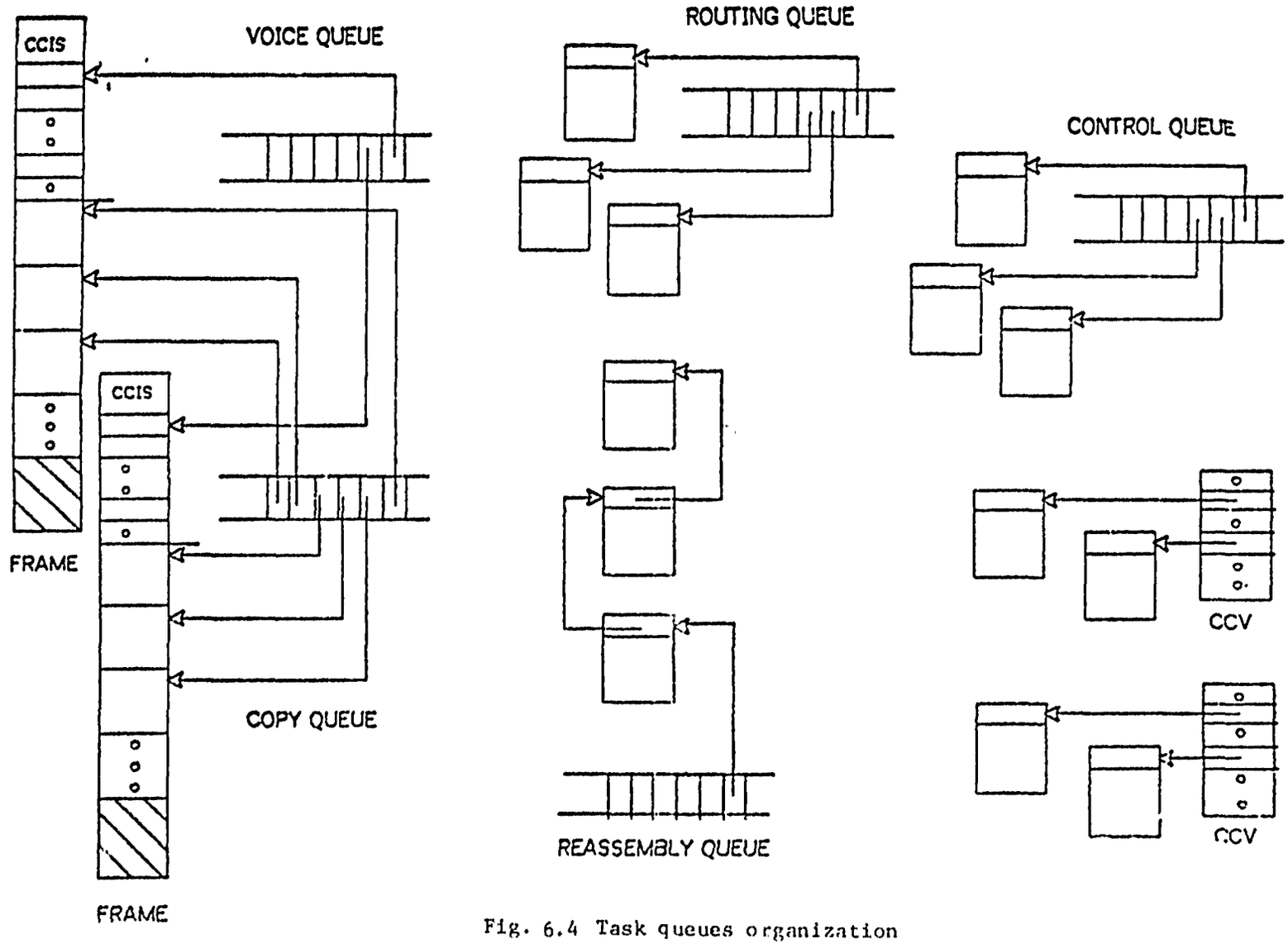


Fig. 6.4 Task queues organization

After the arrival of a frame, the available processor initiates the task of decomposing the frame giving special consideration and precedence to Class I traffic. The handling of incoming Class I traffic by the switch program at a trunk node is basically a "scatter-write" operation where the Class I slots arrive in a contiguous buffer and are copied one part at a time to various output buffer locations as resolved by the Class I routing tables.

The type of design discussed above has possible drawbacks of slippage or overwrite of Class I slots. The first problem consists of the introducing of random gaps when Class I slot misses its output frame and is delayed by one extra frame period. The second problem happens when a Class I slot is over-written by the slot arriving in the next frame and before the output frame has been transmitted. These problems can be avoided by utilizing an extra buffer so that an input frame is never switched to a new buffer in mid-stream.

The Class II packets are individually isolated during the frame decomposition and the Class II copy task queue is utilized to indicate each individual packet. After the termination of the frame decomposition, the processor returns to the pool of available idle processors and computer for the pending tasks.

Fig. 6.5 indicates the sequence of tasks in the integrated switch system. Q_0 is the Input Frame Queue, Q_1 is the Class II Copy Queue. The Class II data packets are copied into individual buffers and thereafter different tasks are created depending on the nature of its type, precedence and final destination (Q_3 and Q_4). Some Class II packets, containing control information or acknowledgements, are forwarded to other switches or a specific control function is performed followed by the packet deletion. Routing and acknowledgement generation tasks are created for the data packets with a foreign destination. The routing tasks are implemented on Q_5 and Q_6.

B. Experimental Design

In C.mmp, two processors are used for both the generation of script (i.e. the incoming frames for each channel) and the analysis of the result. A ring of eight buffers are reserved for each channel.

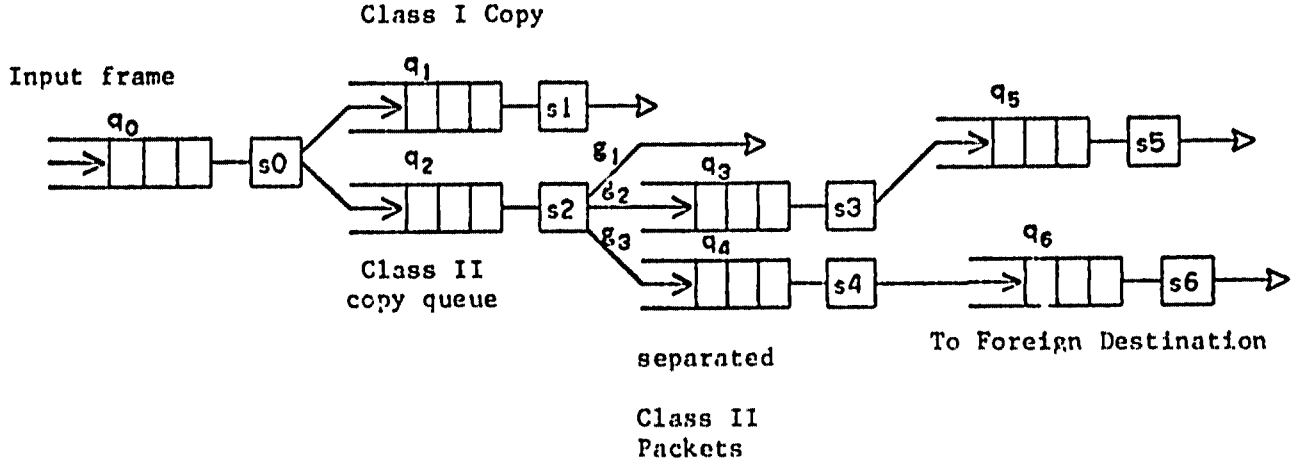


Fig.6.5 Task sequence organization

The analysis process examines all the Class I slots and all the packets sent on each frame, for each output channel. In addition a programmable timer supported by the operating system HYDRA, provides precise timings of frame duration, arrival times, ect. The simulation program is not allowed to use the timing interrupt. But polling by each "slave" processor (the ones carrying out the simulation) allows checking of any interrupt signal.

A separate processor is assigned as a Script Driver to simulate the traffic to the node. The traffic is generated according to the specifications given at the time of the initial set-up. A programmable hardward clock together arrival and departure of frames and other events. These interrupts are serviced by idle system processors.

The parameters for node and the traffic nature can be specified as:

1. Node/Network Parameters - The parameters that can be specified for node and the traffic nature are as follows:
   a. Number of lines connected to the node. A "soft" limit of 4 channels is assumed, mainly for buffer allocation purposes.
   b. Frame duration (typically 10 msec.), relative arrival and departure times of frames on every line. This information is used for initializing and directing the hardware clock routine as to when and which interrupts to post.
2. Line Parameters - Each line is characterized by:
   a. Speed in Kilobauds.
   b. Composition of the real time packets (i.e. length and destination of all real time slots)-In this set of experiments the duration of the run is kept much smaller than typical holding times of real time traffic. Hence the reservations for these are preset and are not changed during the run.
   c. Composition of the Class II and III traffic region-There are twenty one levels of priorities in Autodin-II specs, however such a large number of levels are

of no interest for experiments, since they make design and analysis of experiments unnecessarily difficult. Therefore only six levels are implemented, and during analysis the larger set can be meaningfully mapped onto them. The six levels are Control, Realtime, Data High, Data Low, Bulk high, Bulk low. The fractions indicated are used as discrete linear distribution for determining type for a packet.

d. Direction of traffic flow-That is destination of packets incoming on this line. Fractions are indicated for every other line, which are used as discrete linear distribution for deciding the destination of packet at random.

e. Average number of data packets per frame and their distribution-A poisson distribution is a good choice for this.

f. Length of packets and their distribution.

3. Additional Parameters - Apart from these above line characteristics the following also need to be specified:

a. How long the system should run?

b. How long the system should run before steady state is obtained and statistics collection can be started?

c. Times for statistics collection relative to frames arrival times.

d. Needs for the random number generator.

During the initial set-up phase of emulation parameters, the script driver allows the uset to set, display and modify parameters specified for a previous experiment.

3. Performance Characteristics

A series of discrete runs with completely independent simulation, is utilized to obtain the experimental results. Initially, the experimental interact with HYDRA to create the necessary processes, I/O connections, etc. After initial set-up the program asks for inputs and thereafter the experiment allows the program to begin and waits until it returns to the terminals to find out where to send the output.

Experimental results have been obtained for various traffic conditions. The effect of the channel skew between the frame arrival and departure times on the average packet delay has been observed and the variations for different number of packets/frame are whown in Fig. 6.6-6.9. These curves have been obtained for the following parameters:

Traffic Type: Data

Line Speed: 1.544 magebits/sec. (T1 carrier)

Frame Length: 10 milliseconds

Number of channels: 2 (full duplex)

Frame Departure Time: 9 msec

Channel 0 Frame Arrival: 1 msec

Channel 1 Frame Arrival: 9 msec

For the same system parameters if real time traffic is used the maximum number of slots that can be transmitted can be given as:

	80 bits/slot	800 bits/slot
1 word/move	31	15
4 words/move	34	19

It can be easity seen that a better system utilization is achieved when large size real time slots are transmitted.

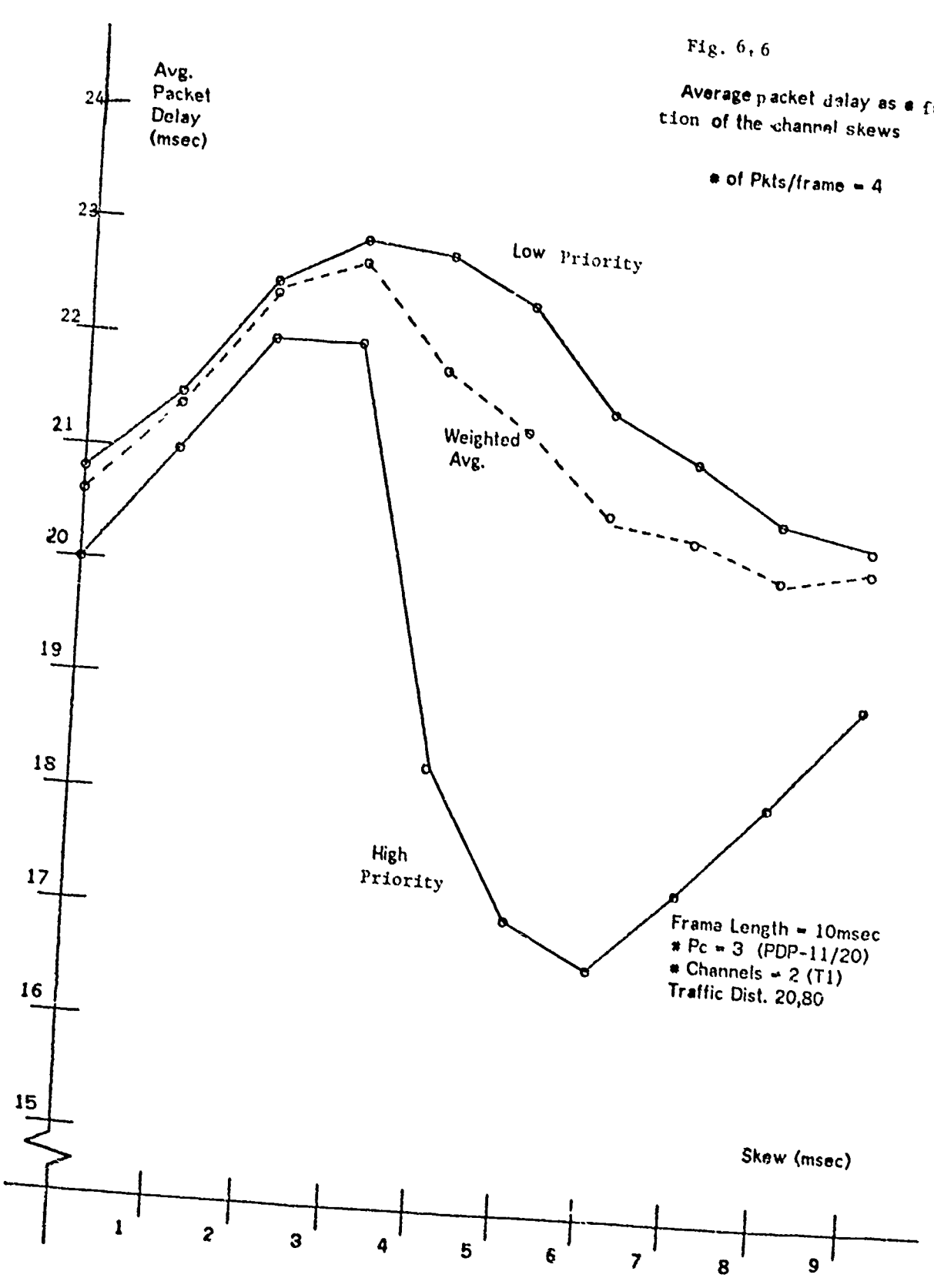
For mixed real time/data traffic, Fig. 6.10 shows the effect of various levels of real time traffic on the average packet delay.

Using different queueing models, the performance of the system has also been evaluated and the results compared. The reliability evaluation of the system has also been done and assuming the failure rates of different parts of the system, the expected life of the system without and with periodic maintenance and an unmaintained Triple Modular Redundant System have also been obtained.

Fig. 6, 6

Average packet delay as a function of the channel skews

of Pkts/frame = 4



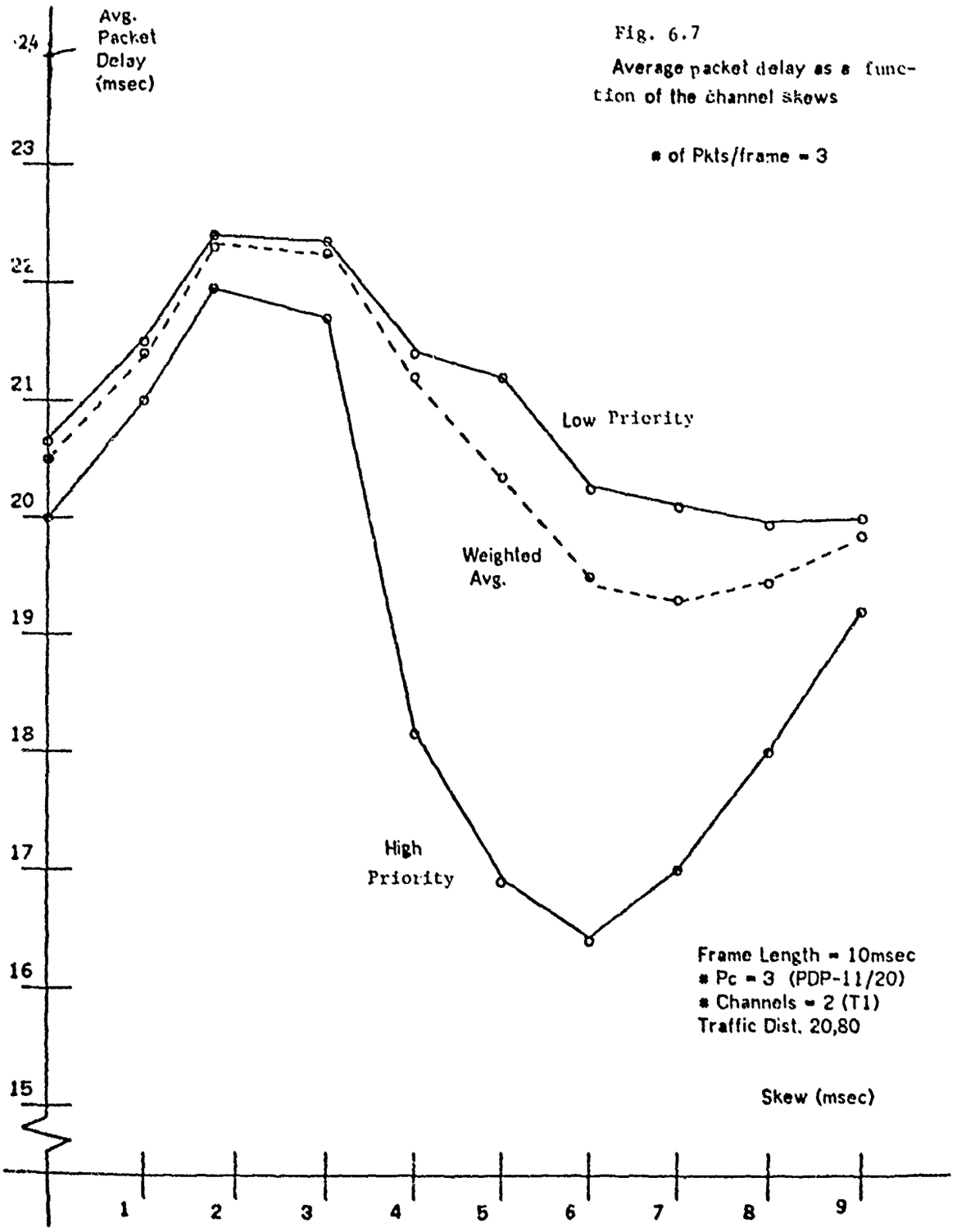


Fig. 6.7

Average packet delay as a function of the channel skews

of Pkts/frame = 3

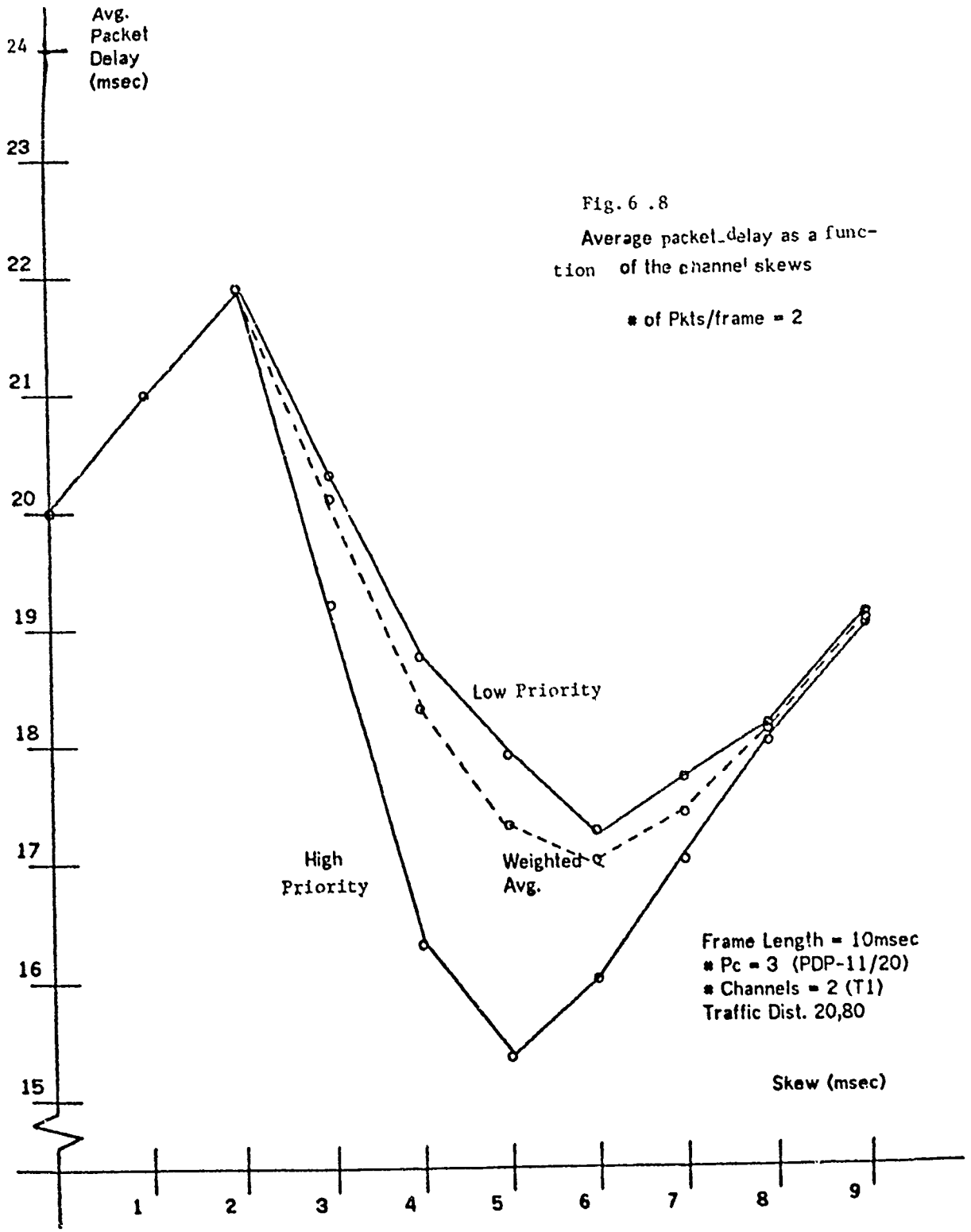


Fig. 6 .8

Average packet_delay as a function of the channel skews

of Pkts/frame = 2

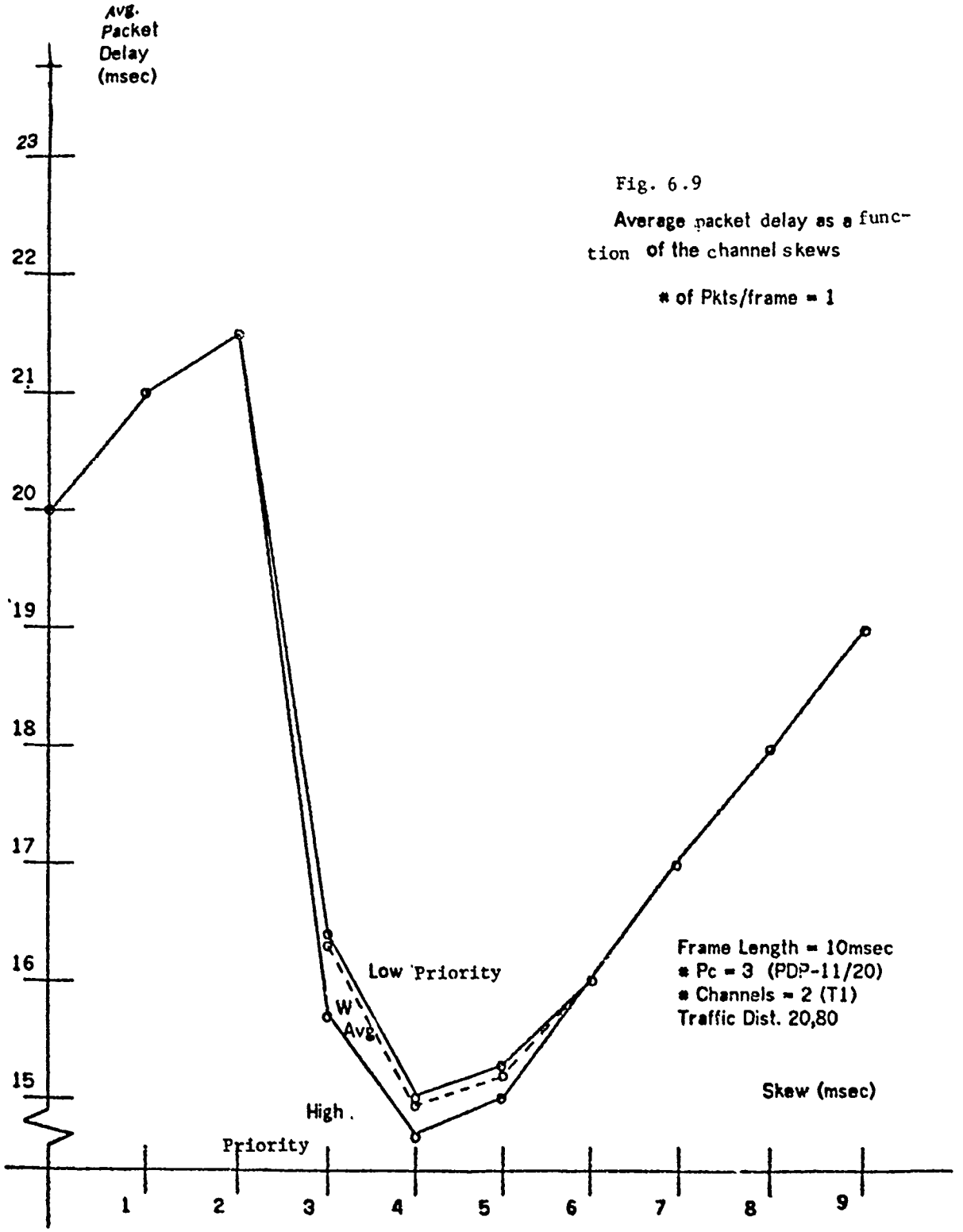


Fig. 6.9

Average packet delay as a function of the channel skews

* of Pkts/frame = 1

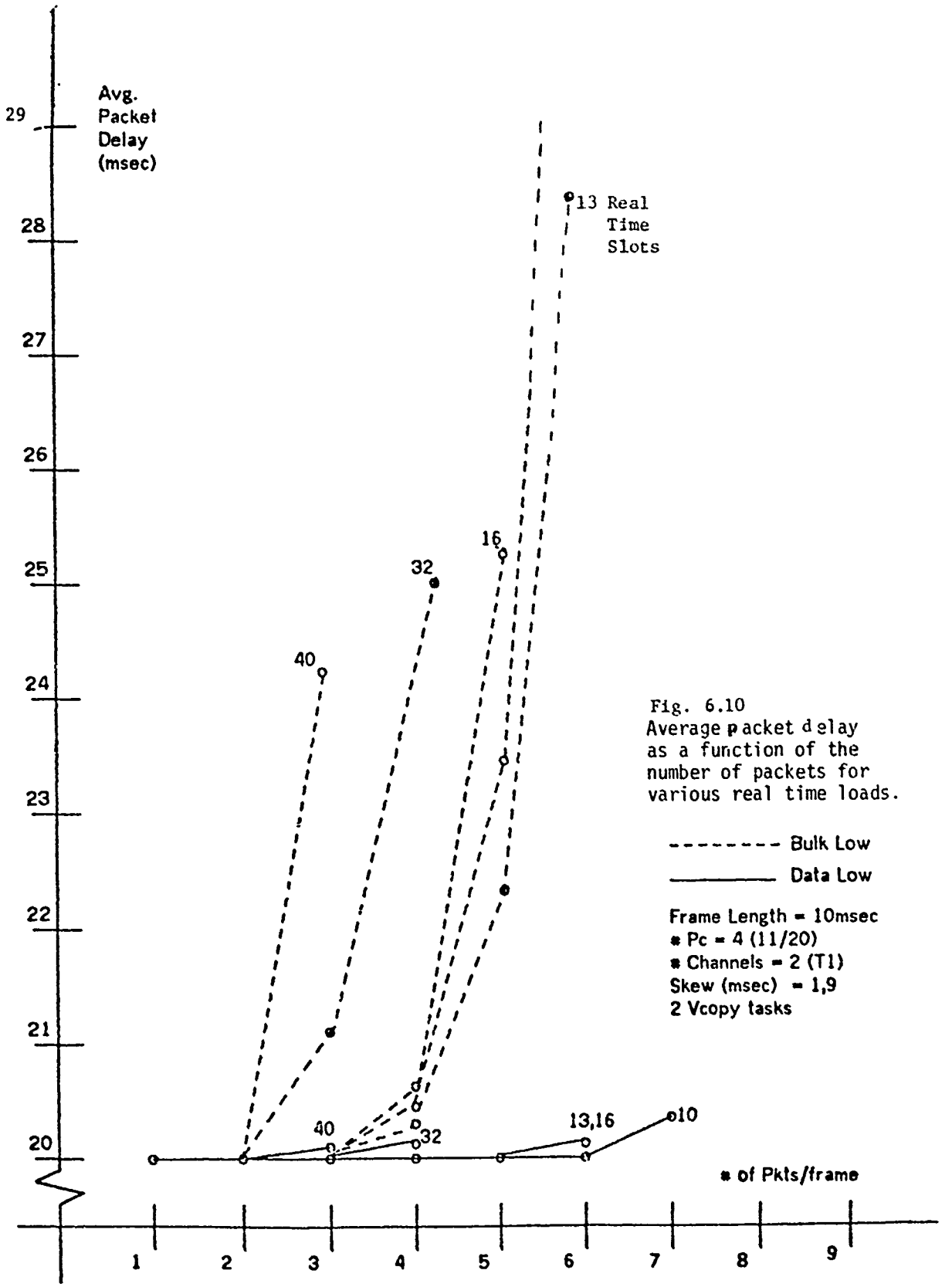


Fig. 6.10
Average packet delay as a function of the number of packets for various real time loads.

4. Discussion

The Carnegie-Mellon reports [19,28] cover in detail the application of multiple processor computer sustems to digital communicatin networks. Much emphasis is given to show the suitability of C.mmp transmission handling of integrated voice and data traffic and possible use of SENET concepts, with minor midifications, has been explored. Several simulation results have also been included. In the absence of any clear indication, we assume that C.mmp is to be utilized as a multi-processor system at each node of the communication network.

The first and most important shortcoming in C.mmp is the use of cross-bar switches for processor-memory interconnection. With 16 processors and 16 memory modules, it is quite unlikely that all 16 processors can be assigned with separate memory modules to do some useful work. Even if we assume that a specific function is assigned to each processor, the memory contention still remains as a major problem. This is true from the fact that the incoming packet(s) are to be stored in successive memory locations utilized as a buffer area. The frame decomposition does not require any data movement, but routing them and reframing of the integrated message to be transmitted to various nodes compels referencing of non-contiguous memory locations. An increasing number of processor necessitates increased switch hardware and a complex control software. Moreover, when a switch fails, there is no way of establishing link to the corresponding functional modules and hence graceful degradation cannot be achieved.

The use of one master processor with a number of slave processors night not be advisable from the fault-tolerance viewpoint. Transmission of CCIS messages : Class I traffic does not provide any error control. The operating system consisting of a kernel and standard extensions is a reliable operating system. But there are other limitations and overhead associated with it. One of such examples is the interrupts to be intercepted by the kernel. The use of higher level abstraction (i.e. processes, semaphores, ports, messages. etc.) is also time consuming for processing of real-time traffic. The time-sharing operating system allows the control of a processor to user on time-slice and periodic scheduling basis.

CHAPTER VII

HONEYWELL ASSOCIATIVE PROCESSING TECHNIQUES

1. Introduction

The objective of the report prepared by Honeywell [21] is to find ways of optimally integrating voice and data traffic with a maximum sharing of the resources. Instead of using conventional processors, the possibility of employing associative and parallel processing techniques in desiging all digital, switched, integrated network has been considered. First, the user requirement baseline is established.

The network user categories are the voice, the narrative/record message, the interactive data and bulk data. Other specific uses are the AUTODIN I, the AUTOVON subscribers, ARPANET-like network and various data terminals. The transmission strategy is on the lines of the SENET concept. Three distinct user classes are:

1. Class I: On Demand, Fixed Delay (voice, facsimile, video),
   Class IA: Noncompressible,
   Class IB: Compressible,
2. Class II: On Demand, Variable Delay,
   Class IIA: Interactive Data, Short Delay,
   Class IIB: Narrative/Record Message, Longer Delay, and
3. Class III: As Available, Variable Delay.

For Class IA - Priority
a. Non-blocking (always accepted)
b. Accepted without delay or blocked with probability of blocking, PB = P_{A1},
c. Accepted without delay or blocked with PB = P_{A2}, and
d. Accepted without delay or blocked, with PB = P_{A3}
e. Accepted without delay or blocked, PB = P_{A4}

where $P_{A1} < P_{A2} < P_{A3} < P_{A4}$.

Classes IB, IIA, IIB, and III are combined into a single precedence structure as shown in Table 7.1.

Table 7.1 Precedence Structure

Precedence Level	Priority	Description
1	0	Control
2	1	Class IB
3	2	Class IB
4	3	Class IB
5	4	Class IB
6	5	Class IB
7	1	Class IIA
8	1	Class IIB
9	1	Class III
10	2	Class IIA
11	2	Class IIB
12	2	Class III
13	3	Class IIA
14	3	Class IIB
15	3	Class III
16	4	Class IIA
17	4	Class IIB
18	4	Class III
19	5	Class IIA
20	5	Class IIB
21	5	Class III

Based on the data rate requirement and the used compression technique, Class I can be divided into the sub-classes of voice (2.4K to 64K data rate), facsimile (4.8K to 300K) and video ($\geq$ 150K). Additional Class I characteristics are:

a. Call lengths are exponentially distributed with a 5-minute mean.

b. Cross network connection time is 3 seconds nominal after completion of call initiation dialogue.

c. Maximum cross network delivery after connection is 250 milliseconds.

d. There is no error control.

e. Blocked calls are lost.

f. Bit count integrity of secure signals is important.

g. All received data streams from access lines at the node are synchronized to the local switch clock.

h. All users are permanently assigned network ports.

i. The initial call dialogue is generally the same for all subclasses.

The Class IIA, the interactive data class, includes terminal-to-terminal, terminal-to-computer, and computer-to-computer communication. The requirements for this class are as follows:

a. Cross network connection time is 30 seconds nominally, with a nominal one-second cross network delivery time.

b. Expected message size is assumed to range from as few as three 8-bit characters plus header up to a maximum of 40,000 characters, with length exponentially distributed and a mean of 2000 bits.

c. A virtual interconnect may last several hours. However, operation is typically half-duplex so that only simplex switching is required as a node; i.e., each direction must be switched independently.

d. Variable input rate is from 75 bits per second to 100K bits per second.

e. Error control is required for each packet in a link-by-link fashion (i.e., not end-to-end) and it required on access lines for all but Class IIA.

f. Bit count is important.

g. Data exchange requirement between terminals and computers requires different interface discipline and protocol at the two ends.

Class IIB - Narrative/record messages are similar to interactive data except the following:

a. Longer connection and delivery times are acceptable.

b. Average message length is 20K bits.

c. All protocols and formats are similar to AUTODIN I.

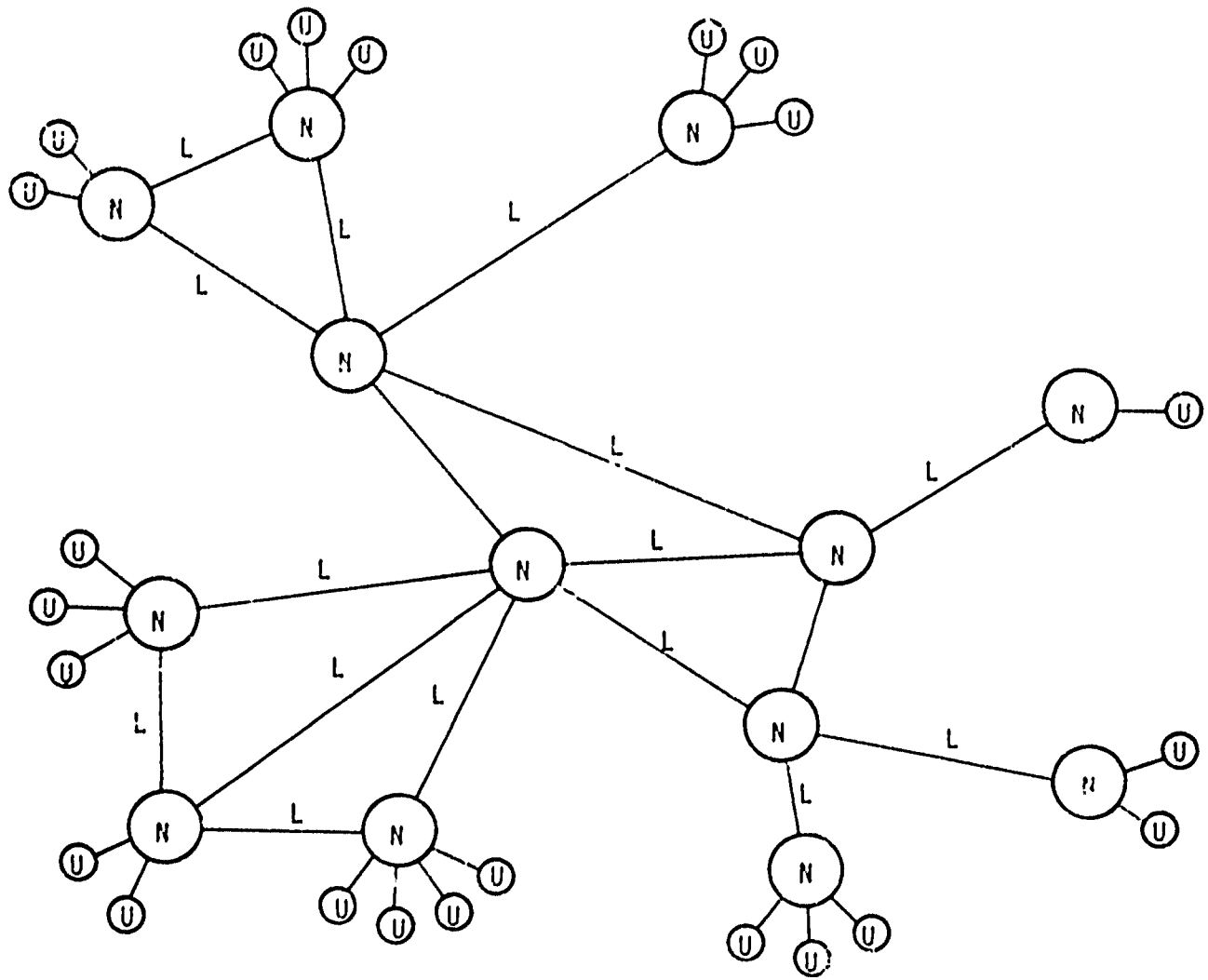
In Class III, bulk data means no real-time response obligation and long messages. The data is generated by the remote batch systems or computer-to-computer transmission. The following are the requirements for this class of traffic:

a. Cross network connection time is 30 to 60 seconds with non-critical delivery times (i.e., from 5 minutes for Bulk 1 and upto 4 hours for Bulk 2).
b. Message statistics are similar to interactive data except that the maximum message size is 10^8 bits with a much higher mean length.
c. Variable input rate from 4.8K bits per second to 1M bits per second is desired.
d. Error control is required. A 32-bit cyclic redundany check (CRC) per packet shall be provided as a minimum.
e. Bit count integrity is important.
f. Line interface discipline is specified by Advanced Data Communication Control Procedures (ADCCP).
g. Addressing and call initiation is similar to that described for Class IIA.

The routing and handling information for the Class I users is specified by the node and the segment leader format thus generated is handled as another input segment. Class II and III formats follow the one specified for the packet switched network. The basic element of information exchange is the segment which is composed of a leader followed by the variable size text. The five acceptable line formats are binary, packet binary, character, canned character, and the character unclassified.

2. Archirectural Description

A typical network configuration composed of nodes and interconnecting communications links is shown in Fig. 7.1. The node structure is depicted in Fig. 7.2. The information to be presented in the form of a binary bit stream is to be transmitted as either line switched or packet switched data. The Class IA traffic is treated as line switched (L/S) while Class IB, Class II and III data is packetized at the source node before being transmitted over the network. The bit stream over a link is grouped into "frames" with a fixed frame time for the whole network. The frame time is kept fixed and depending on the speed of a link, it contains a fixed number of bits. A frame consists of a Start-of-Frame



N: Node
U: User Access
L; Link

Fig. 7.1 Network structure.

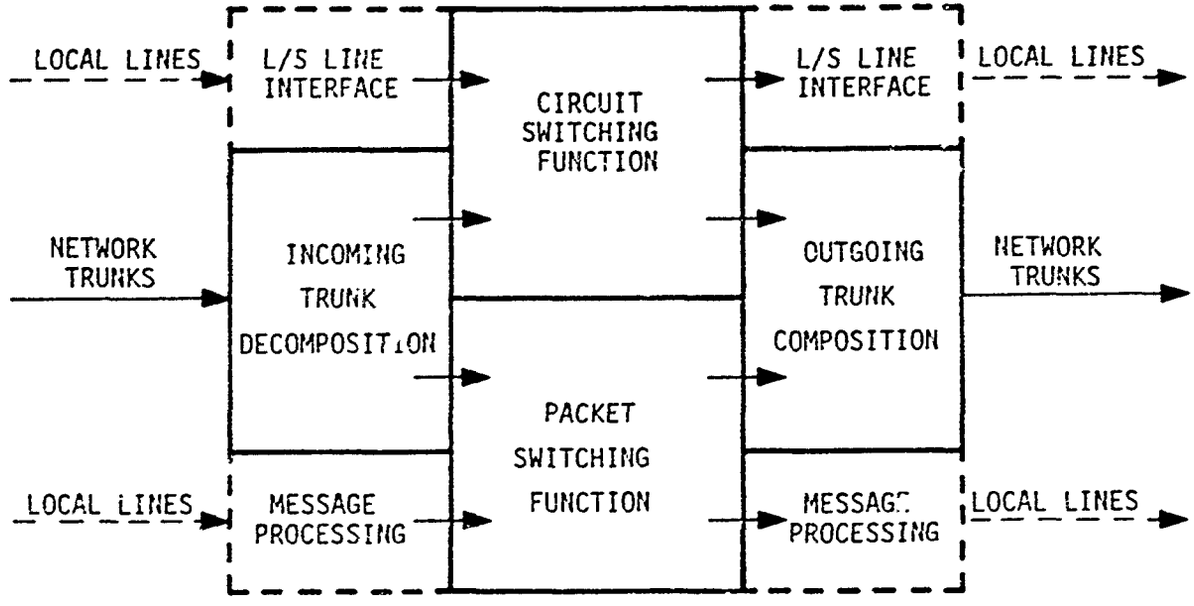


Fig. 7.2 Node structure
(Honeywell integrated voice/data switching).

marker (8 bits), a Transition-Synchronization Field and a number of variable-size slots for L/S and packet data transmission and is shown in Fig. 7.3.

After an L/S call setup, variable size slots are allocated for it and remain unchanged for the duration of the call. For an L/S call, a best fit algorithm is used to minimize the number of slots required per call. The unused slots within the frame is filled in by the Packet Data. Each packet is delimited in front by a bit sequence called a flag. A typical packet distribution is shown in Fig. 7.4.

Communication between nodes is achieved via a communication link existing between a pair of nodes. The sending node acts as the line master (Fig. 7.5) and the format and content on the line is determined by the transmit table resident in the master. One such table is illustrated in Table 7.2. Two different approaches of the Frame Synchronization are also discussed. An accurate time slot transitioning from packet-switched data to line-switched data or vice versa, is obtained by the use of a network control packet and a synchronization field. The packet switched data are divided into the following four types:

a. Data packets (ClassII/III user data),
b. Control packets (for Class 1A/1B call setup, takedown, or for Class II/III data transmission procedures),
c. Acknowledge (ack) packets, and
d. Voice packets (Class 1B - clear voice - call 10-ms samples).

Five types of control packets for handling L/S call setup and takedown are:

a. L/S Slot reservation command/request,
b. L/S Slot reservation command,
c. L/S Slot reservation request denied,
d. L/S Slot unreserved command, and
e. L/S Slot de-reservation command.

The P/S Transmission is handled by the following control packets:

a. P/S transmission connection request,
b. P/S transmission connection answer,
c. Multi-packet transmission request,
d. Ready to receive multi-packet message, and
e. Confirm acceptance of a single-packet message.

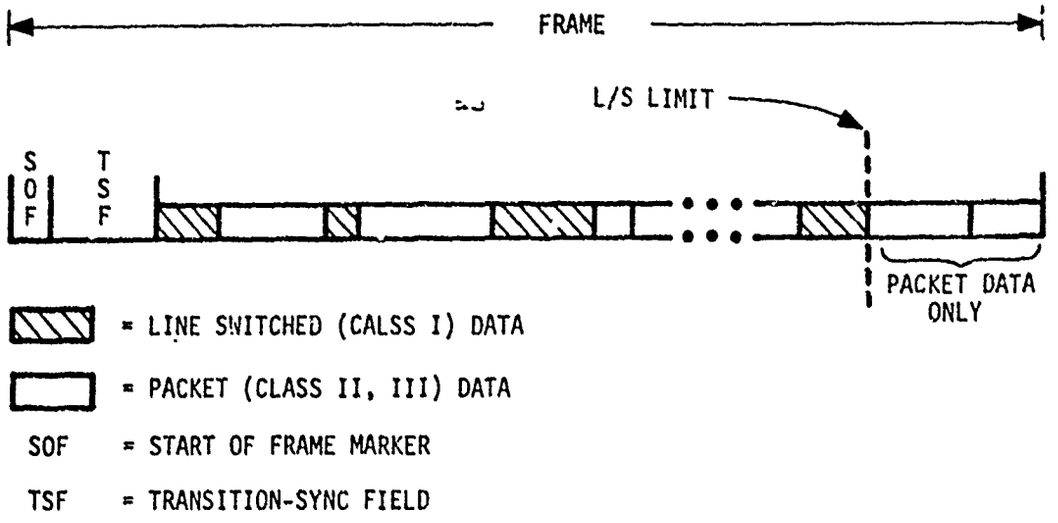


Fig. 7.3 Line switched/packet data integration.

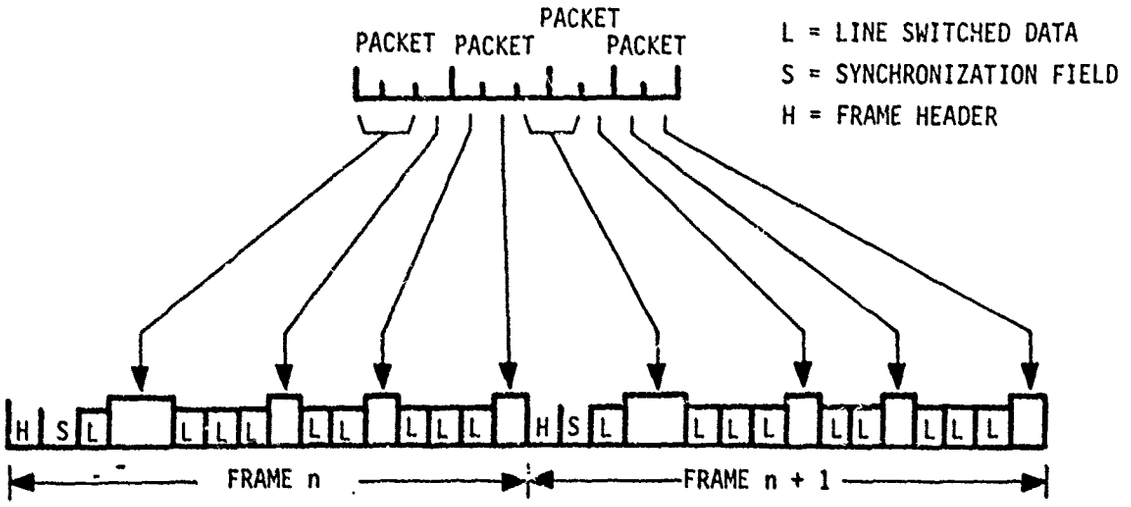


Fig. 7.4 Packet distribution.

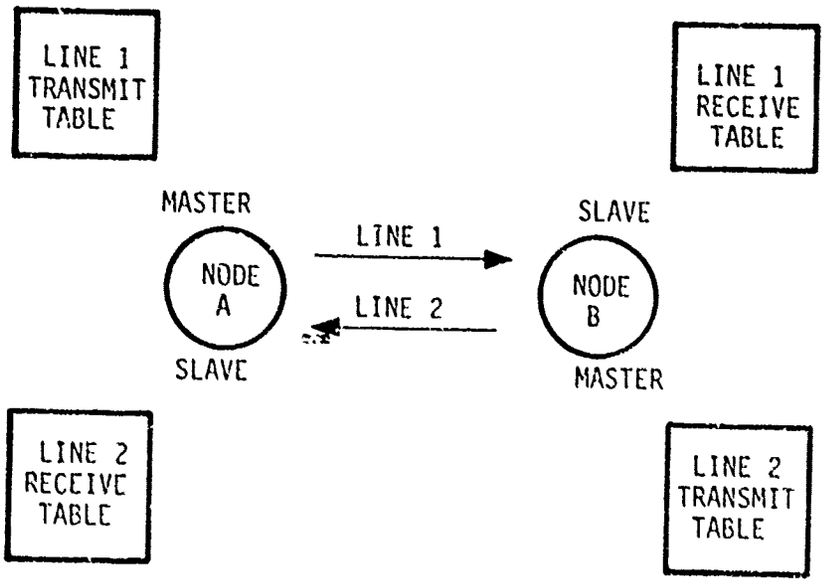


Fig.7.5 Network Link.

Table 7.2 Transmit Table

	State	Starting Byte	Size	L/S Call No.	Buf No.
P/S	00	25	1864		
L/S	11	4	6	87	211
P/S	00	20	2		
L/S	11	22	3	9	110
L/S	11	10	10	38	96

The main communication oriented architectural concepts allowing transmission of integrated traffic are now discussed below:

A. Line-switched call setup/takedown procedures

The line-switched call setup/takedown procedures consist of slot reservation (de-reservation) and allocation (de-allocation). The steps for these are also considered.

The eight node processes are functionally defined as:

a. frame decomposer,
b. control packet processor,
c. synchronization field processor,
d. control packet formatter,
e. receive table updater,
f. transmit table updater,
g. L/S router, and
h. frame composer.

The frame decomposer separates incoming frames into the synchronization field, L/S field, control packets, data packets and the voice packets. It receives input from the incoming communications line, the receive table and the Node Control.

The control packet processor interprets control packets and requests the receive table updates, transmit table updates and the route selection. The synchornization field processor responds to other network nodes.

The receive table updater responds to queued requests for updating the receive table to indicate the L/S call setup, L/S call takedown and L/S call pre-emption. Similarly, the transmit table updater takes care of updating the transmit table to reflect the L/S call takedown and L/S call pre-emption. The frame composer creates outgoing frames by combining elements from the output data packet queue, output voice packet queue, L/S data, output control packet queue and the synchronization (sync) field data.

The process flow sequence, i.e. the sequence of actions to be taken by a node in response to the receipt of network L/S control packets and valid synchronization fields are also outlined.

B. Packetized-Voice (P/V) Call (Class IB) Setup/Takedown Procedures

Similar to Class IA invoice call, special control packets are used to set up a P/V call by establishing a fixed route. The trunk space is reserved according to the Class 1 data limit. A P/V call switching table is used at each node to allow switching of a fixed output trunk. The updating of the call table is the only function to be performed at the node. The call setup procedure and the corresponding flow chart are also given.

C. Packet-Switched (P/S) Data Transmission Procedures

The packet transmission procedure between source node and destination node are:

a. Source to Destination Node Protocol for Class II/III
   i. Connection setup between source node and destination node,
   ii. Multi-packet message transmission procedures,
   iii. Single-packet message transmission procedures.
b. Source-to-Destination Node Protocol for Control Packets, Acknowledgement (Ack) Packets and Voice Packets.
c. Node-to-Node Packet Protocol.

The details for each one of them may be found in the report [21].

D. L/S and P/S Routing Considerations

The L/S and P/S routing considerations are analysed in the areas of routing data base, line switched routing and the packet routing. Routing of packets and line switched calls require that each node must have a data base describing the node and network structure and the dynamic node and network status. The first data base includes the number of lines and trunks, the length and capacity of each line or trunk, the queue and buffer capacities and the deterministic factors. The dynamic node and network structure data base includes the queue and buffer occupancy, the precedence of call and packets, the age of queued packets and the predicted transmission times.

The line switched routing considerations include the following criteria:

a. route selection criteria,
b. alternate route selection, and
c. back routing.

The packet routing process consists of:

a. selection for routing,
b. route selection, and
c. selection for transmission.

E. Nodal Structure

Suitable hardware is needed for the nodal data part structure and the L/S call functions and the structure for P/S call functions.

A nodal data path structure that fulfills the integrated network functional requirements is given in Fig. 7.6. It contains a fixed-delay switch, packet storage and node control. The node control maintains the receive table which provides the decomposition of frames received at incoming node-to-node trunks. Packets selected for re-transmission are moved to a storage area associated with the selected outgoing trunk. The composition of a frame by line-switched data from the fixed delay switch and packet-switched data from storage is done by utilizing the transmit tables. Local access is provided separately.

An associative call-buffer switch is developed to perform the L/S call (Class IA) switching function at each node. Such a switch including the frame decomposition, L/S data switching and frame composition is shown in Fig. 7.7.

On the receiver side the frame decomposer and data distributor (FDDD) for each trunk performs these operations:

a. distributes the received Frame Header and sync Field (FHSF) into the FHSF input buffer for further processing,
b. distributes the packet data (including all four packet types, such as data, control, ack, and voice) into the P/S input buffer for further processing, and
c. associatively distributes L/S data (Class IA) into individual FIFO buffers where each FIFO buffer has been assigned to one L/S call.

On the transmit side the reverse operation is performed.

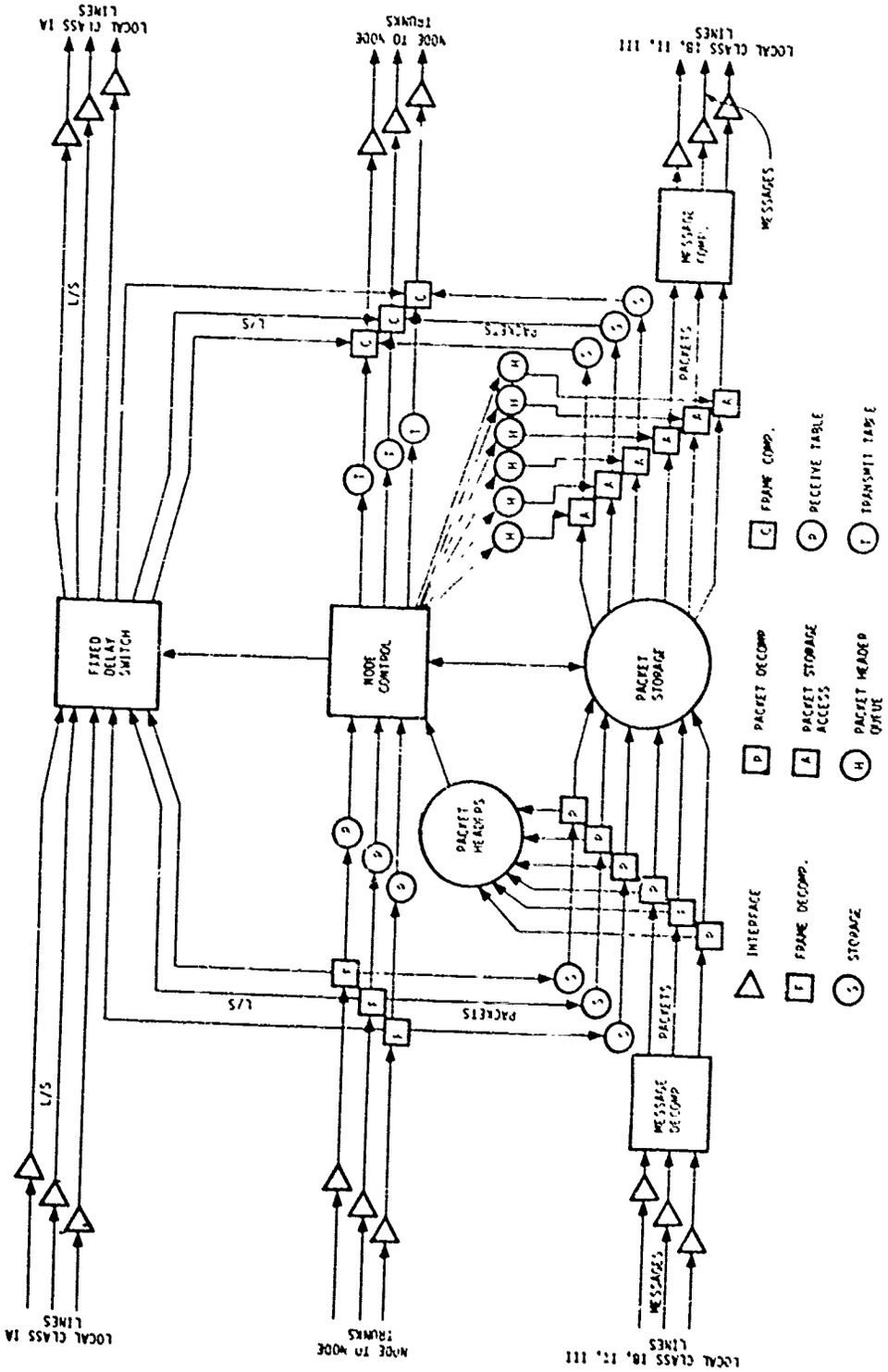


Figure 7.6 Nodal data path structure

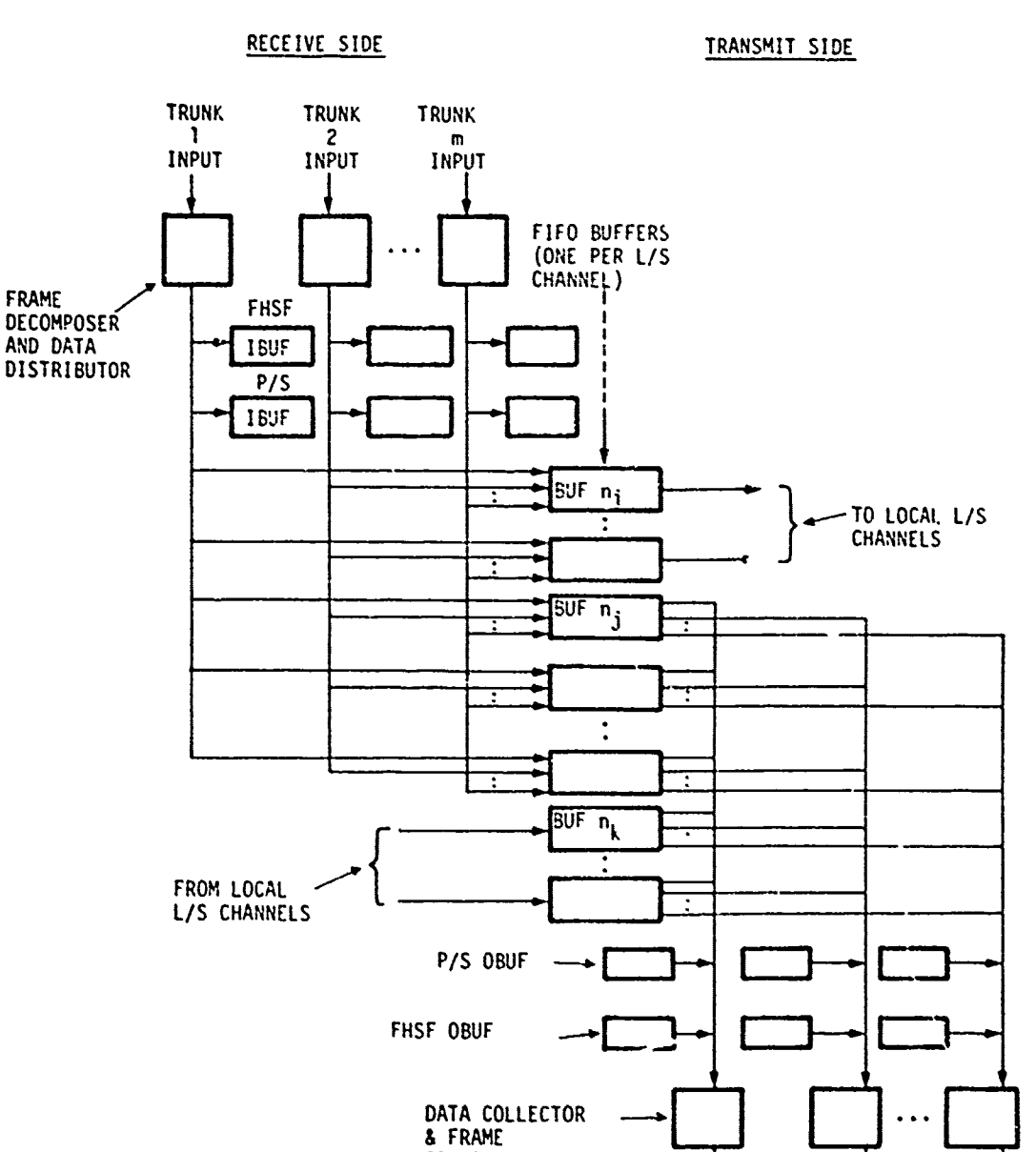


Fig. 7.7 Node data flow -- Decomposition, switching, composition.

In each FDDD, an associative memory transmit/receive table is used for frame composition/decomposition and for line-switching related information. It is also employed to switch L/S data to and from the correct call buffer. L/S call slot reservation/de-allocation is also done using Associative Memory (AM) Transmit/Receive Table.

3. Performance Characteristics

The main constituents for processing Class 1A (non-clear-voice) calls at a node are the AM transmit tables (one per trunk), the associative gating logic at the transmit side, the AM receive tables (one per trunk), the associative gating logic at the receive side, and the FIFO buffers (one per L/S call through the node). To obtain the size and quantity requirements of these components, the following parameters are assumed:

a. 16 T1 carrier trunks at a node,

b. maximum 85% Class 1 data on trunks,

c. among Class I data, 70% are Class 1A (non-clear-voice) and 30% are Class 1B (clear-voice),

d. data rate distribution for Class 1A data,

   i. 25% with rate 64 Kdps ~ 300 Kbps,

   ii. 50% with rate 9.6 Kbps ~ 56 Kbps,

   iii. 25% with rate 2.4 Kbps ~ 8 Kbps,

e. on the average, 1.5 slots in the frame for each L/S (Class 1A) call, and

f. frame size is 10 msec equivalent (i.e. 15440 bits with T1 rate).

These figures lead to the following node requirements:

a. Associative Memory Tables

   i. Number: 32

   ii. Size: 200 words x 50 bits

b.

FIFO Buffer Size	No. of FIFO Buffer
i. 3000 bits	58
ii. 560 bits	462
iii. 30 bits	770
Total	1290

The buffer size is obtained for the highest data rate call in each category. For T1 trunks and 10 ms frame time, each input buffers a new bit every 647 ns. If ten bi-directional trunks access a single memory, the memory bandwidth has to be over 15 megabits/second- If bit serial reading and writing is utilized, a 33 ns cycle time in required. The common packet storage(PS) cycle time for various word size is given in Table 7.3. Alternately, the number of trunks that can be supported by various word-size 500 ns memory is shown in Table 7.4.

The modularity and expandability of associative memories and LSI implementation feasibility are also emphasized. The nodal packet switching mechanism is also discussed. Suitability of the Honeywell Associative Multi-Access switch for the functional implementation or the cross-switch path connection is also investigated.

4. Discussion

The Honeywell report illustrates an excellent way of utlizing associative techniques whenever decisions have to be taken based on the instantaneous contents of a table. The simultaneous complex search capability inherent in the associative memory organization allows fast table look-up and maes the routing process much faster. The associated pointers make decompositon/composition of a packet also easier. The basic organization of the nodal data flow structure also looks attractive, convenient and efficient.

One of the main shortcomings of the proposed organization is the implementation details of buffers. As there should be provision for a link between on input buffer and any output buffer, the design needs a careful attention. The reliability and graceful degradation aspects are missing from the report. The processing requirement at each node is not well defined.

The packet switching concept has been covered in detail. But no account is fiven on how circuit switching at the node level is achieved. The size requirement of the packet storage and implementation of the node control have not been covered in

Table 7.3 Required PS Cycle Time for a Node with Ten Bi-Directional Trunks.

Word Size	PS Cycle Time
1 bit	33 ns
8 bits	264 ns
10 bits	528 ns
32 bits	1056 ns

Table 7.4 Trunk Capacity for a Node Utilizing a PS Memory with a 500 ns Cycle Time

Word Size	No. of Bi-Directional Trunks
1 bit	0.6
8 bits	5.2
16 bits	10.4
32 bits	20.7

detail. It is also important to cover the hardware and software diagnostic techniques.

CHAPTER VIII

RCA CORPORATION UNIFIED NODE APPROACH

1. Introduction

The RCA report [30] has emphasized the concept of a Unified Node with Dynamic Channel Allocation as a means of providing integration of circuit switch, message switch and packet switch functions within a single node. This allows composition of the internodel trunks which contain digitized voice time slots and non-real time data multiplexed in a frame structure. A modular, versatile node supports the following functions:

1. providing for secure and non-secure circuit switching of Class I traffic,
2. accommodating a wide variety of Class I traffic, such as variable rate digital voice subscribers, high speed FAX, slow scan TV, and interactive graphics,
3. providing for message store and forward switching to handle narrative record traffic,
4. providing for packet switching to handle asynchronous but near real time data transactions to accommodate the following needs:
   a. man/man (terminal/terminal) communications including both interactive type communications and standard narrative/record communications,
   b. man/computer (terminal/computer) query response communications,
   c. computer/computer communications ranging from transfer of short interactive traffic to transfer of very lengthy transaction (bulk),
   d. CCIS signalling for establishment and disestablishment of Class I calls, and
   e. Class II control messages to control packet and/or message accountability, flow control, configuration control, transfer of statistics, etc.
5. provide for Dynamic Channel Allocation. A key feature of the node is to provide for a single type wideband trunk which can contain all classes and types of traffic multiplexed in

a highly efficient fashion. These trunks will be the sole means for internodal communications and offers the following advantages:

a. use of few wideband trunks as opposed to many narrow-band trunks should offer significant advantages in terms of rental costs, and cost for design and maintenance of the tech control subsystem,

b. many different data rates of Class I traffic may have to be accommodated by the node. Ability to compact traffic on internodal trunks by providing for proportional size channel slots in the multiplexed frame permits efficient utilization of the transmission facility,

c. a reduction in transmission efficiency and a significant improvement in non-peak hour performance is achievable by permitting data to be transmitted over unoccupied voice channels.

The Unified Node Message Switching with the users is indirectly achieved via the packet switching in the node. The Circuit Switching is controlled by the processor. The packet switching flow control between the source and destination is done by utilizing the necessary control and routing information contained in the packet. To handle various types of traffic, the central control provides the following nodal functions:

1. node configuration and load control,
2. traffic and routing control,
3. performance assessment and status monitoring,
4. fault diagnoses,
5. patching and testing, and
6. communication with a network control center.

2. Architectural Description

The architectural considerations for the unified node are elaborated in the following subsections:

A. dynamic channel allocation,

B. common channel information signalling,

C. node architecture-hardware,

D. node architecture-software,

E. interfacing the ADPT testbed to existing networks, and

F. ADPT testbed and experiment descriptions.

These are summarized in the paragraphs below:

A. Dynamic Channel Allocation

Efficient integration and multiplexing of all three classes of traffic onto the internodal trunks are to be done at the node. Various possibilities for handling Class III traffic have been considered and processing of Class III bulk data as lower priority Class II packets has been suggested as the best solution. The delimiter between Class I and Class II data is seen to be non-essential and the individual boundaries are determined by the programmed limits.

Class I traffic rates, traffic delay, transmission efficiency and the storage requirements are the important factors involved in determining a suitable frame structure. It has been concluded to have 100 frames per second by using T1 trunks (1.544 MBS rate) with a frame size of 15,440 bits. The multiplexed frame structure is shown in Fig. 8.1.

Allocation of different slot sizes allows mixing of Class I call rates. The termination of the frame without completing transfer of the Class II final packet in transit improves the transmission efficiency. The buffering of digitized voice introduces the transmission delay. This delay as a function of frame rate and number of nodes is shown in Fig. 6 '. Bandwidth limitation for Class I and Class II data within the frame is also desirable.

The following problems in dynamic channel allocation needs careful attention:

1. synchronization of basic multiplex frame,
2. maintaining synchronization of the frame during dynamic channel changes, and
3. maintaining bit integrity on the synchronous data channels.

The dynamic channel allocation has the impact on the system

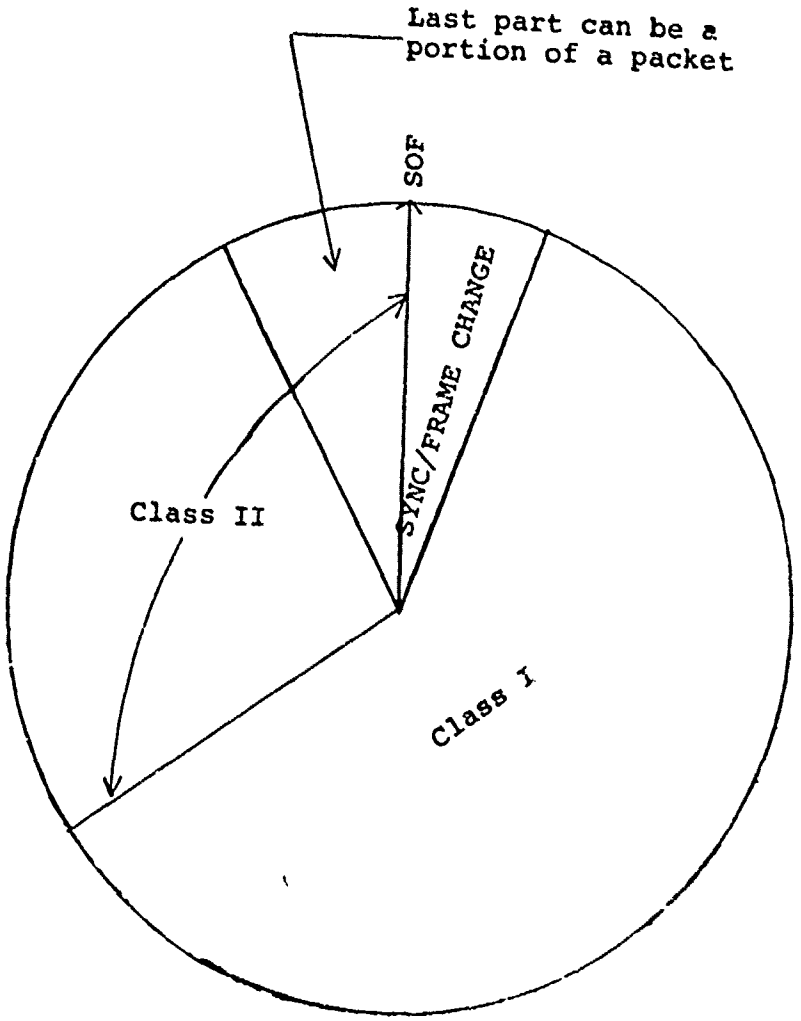


Fig. 8.1 Frame without Class III traffic.

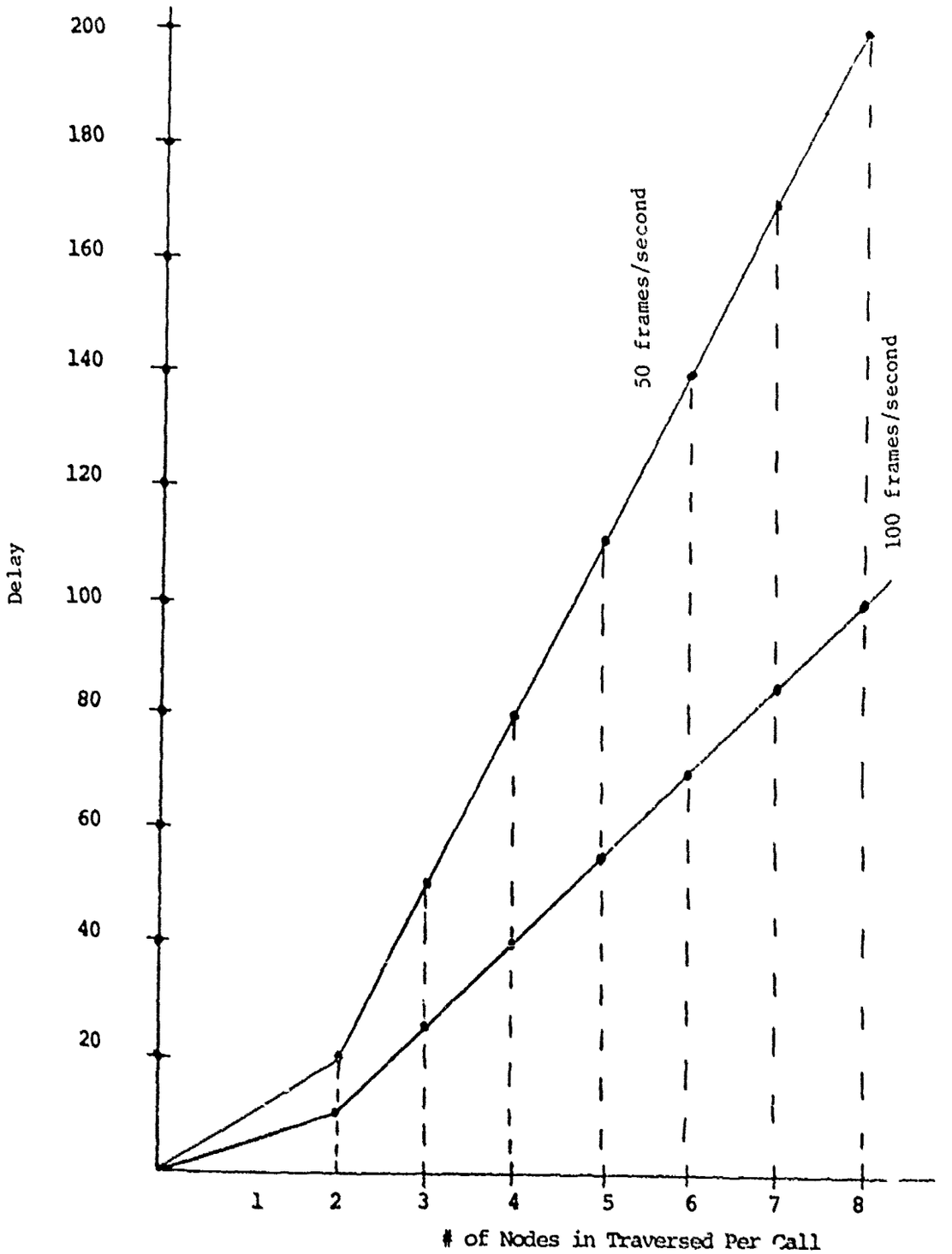


Fig. 8.2 End-to-end Class 1 traffic delays.

aspects such as:

1. priority/preemption:
   a. Priority I - CCIS messages, network control messages and highest precedence data traffic,
   b. Priority II - interactive data traffic, and
   c. Priority III - bulk and narrative record traffic;
2. security,
3. routing,
4. call setup and breakdown,
5. service features,
6. technical control, and
7. network management/control.

The key advantages of the dynamic channel allocation concept are:

1. the ability to efficiently accommodate a wide range of data rates,
2. the ability to reduce the transmission bandwidth required in the network,
3. reduction in technical control, modem and crypto costs are realized by multiplexing with the switch,
4. it is obvious that the ability to satisfy varied user requirements with a single system results in reduced acquisition, production and life cycle costs (when compared against using independent switch networks for different type user group). A specific cost trade study will be required to determine detailed cost savings.

B. Common Channel Information Signalling (CCIS)

Several approaches for CCIS information transfer have been considered and transmission as asynchronous data packets with highest priority is observed to be the best approach. The frame changing is to be done at both coordinating ends (i.e. sending and receiving ends) of the link at the same time. The conflict situation of both the switches simultaneously trying to change the trunk frame can be easily resolved by the master/slave approach. All queued CCIS message requests are concatenated to form a single frame change command packet. The suggested sequence is as follows:

1. Slave sends call requests to master as they arrive.
2. Master accumulates its own and the slave requests and prepares and transmits the concatenated packet.
3. The slave acknowledges the receipt and declares it to be ready for frame change.
4. Master initiates frame change sequence.
5. Slave responds with frame change sequence.

The unified node sends a variety of signalling and supervisory messages such as:

1. voice CCIS (Class I traffic),
2. data and control messages (Class II traffic),
3. network management messages, and
4. system control messages.

The packet link control described in the Advanced Data Communications Control Procedure (ADCCP) is to be adopted for Class I message formats. For Class II traffic, the control message formats are shown in Tables 8.1 and 8.2.

C. Node Architecture - Hardware

A nodal architecture capable of providing the user services has to be defined by analyzing the requirements of the future node. The data traffic and digitized voice communications are expected to increase substantially in future and hence the two key factors to be considered in node architecture are the flexibility and modularity. Three classes of digital traffic to be allowed and the nodal switching capabilities to be included are the circuit switching, the store and forward message switching, the packet switching and the bulk data service. The following subscribers have to be accommodated:

1. Voice Subscriber Lines:
   a. Standard Analog Phones,
   b. AUTOVON Switch Trunk,
   c. TRITAC and DAX Switch Trunks,
   d. Digital Non Secure and Secure Phones (DSVT,DNVT);
2. Synchronous Data Sources:
   a. FAX,

Table 8.1 Packet Data Call Header

1. Format Identifier
2. Packet Type/Security
3. Destination Node
4. Net Address (Destination Line)
5. Destination Line
6. Packet Sequence No.
7. Route Controls
8. Network/User Controls
9. Route Tabulation (indicating Network passed)
10. Route Tabulation (indicating Node Group passed)
11. Route Tabulation (indicating Node Unit passed)
12. Logical Channel
13. Precedence/Security
14. Transmission Control Code (TCC)
15. Originating Node
16. Originator Network
17. Origination Line
18. End of Header Symbol (EOH)

Table 8.2 Packet Response

1. Format Identifier
2. Packet Type
3. Destination Node
4. Net Address/Destination Line
5. Destination Line
6. Allocation
7. Route Controls
8. Net/User Controls
9. Route Tabulation (Network)
10. Route Tabulation (Node Group)
11. Route Tabulation (Node Unit)
12. Logical Channel
13. EOH

b. Video,

c. On Line Graphics (i.e. Light Pen Terminals, Optical Readers);

3. Asynchronous Data Sources:

a. Mode IIA data (i.e. TTY),

b. Mode I data (i.e. AUTODIN, DSTE), and

c. Mode VI (ADCCP) data (i.e. intelligent terminals, host computers).

The node size is dependent upon the amount of traffic to be handled. The node size requirements in 1985 and beyond, are shown in Table 8.3. It clearly shows that a super node has to handle 16 times the traffic of the small node. A simplified functional block diagram of a unified node is illustrated in Fig. 6.3. The packet switch functions include the following:

1. link access protocol,
2. segment validation,
3. segment/packet format conversion,
4. source node call control,
5. packet route,
6. packet validation,
7. destination node call control,
8. packet/segment conversion,
9. setment transmit,
10. packet transmit, and
11. CCIS message processing.

The node processing system can vary from a single processor to a large multi-processor array. A large packet throughput is to be achieved by allocating bit and byte handling functions to the front end hardware. A modified single processor is shown in Fig. 8.3, The Interactive Communications Channel (ICC) allows interfacing of multiple real time data links. Data transfer to/from buffers to the memory is done via the direct memory access technique. The ICC hardware and software functions are:

1. Hardware:

a. poll interface lines for data,

b. detect/generate framing characters,

Table 8.3 Node Sizes

Voice Traffic Load

	Small	Average	Large	Super
Load	70 Erlangs	235 Erlangs	625 Erlangs	1125 Erlangs
Lines	200	600	1200	2400
Trunks	100	280	670	1160
Average Thruput	4.48 MBS	15 MBS	40 MBS	72 MBS
Max.	6.4 MBS	18 MBS	42.8 MBS	74.2 MBS

Data Traffic Load

	Small	Average	Large	Super
Load	80 P/S 160 KBS	270 P/S 540 KBS	720 P/S 1.44 MBS	1300 P/S 2.6 MBS
Average Thruput	320 KBS	1.08 MBS	2.88 MBS	5.2 MBS
Peak Second	736 KBS	2.48 MBS	6.62 MBS	11.96 MBS
Lines	70	210	420	840
Buffers for Packets	42,500 Bits	130,000 Bits	346,666	626,000 Bits
Tables	2,000 Bits	6,000 Bits	12,000	24,000 Bits
Program Size	12,000 Bits	12,000 Bits	12,000	12,000 Bits

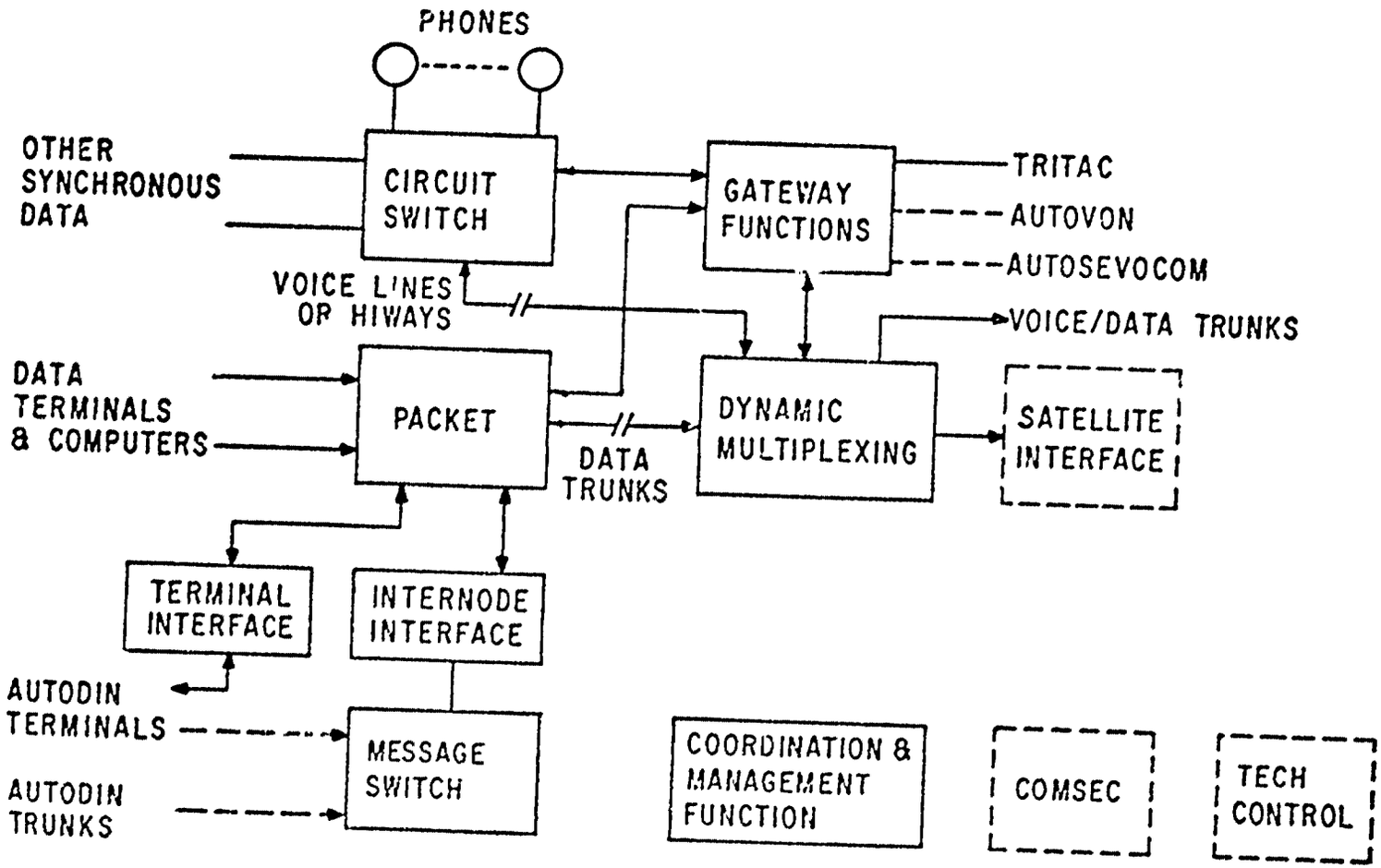


Fig. 8.3 Unified node functional block diagram

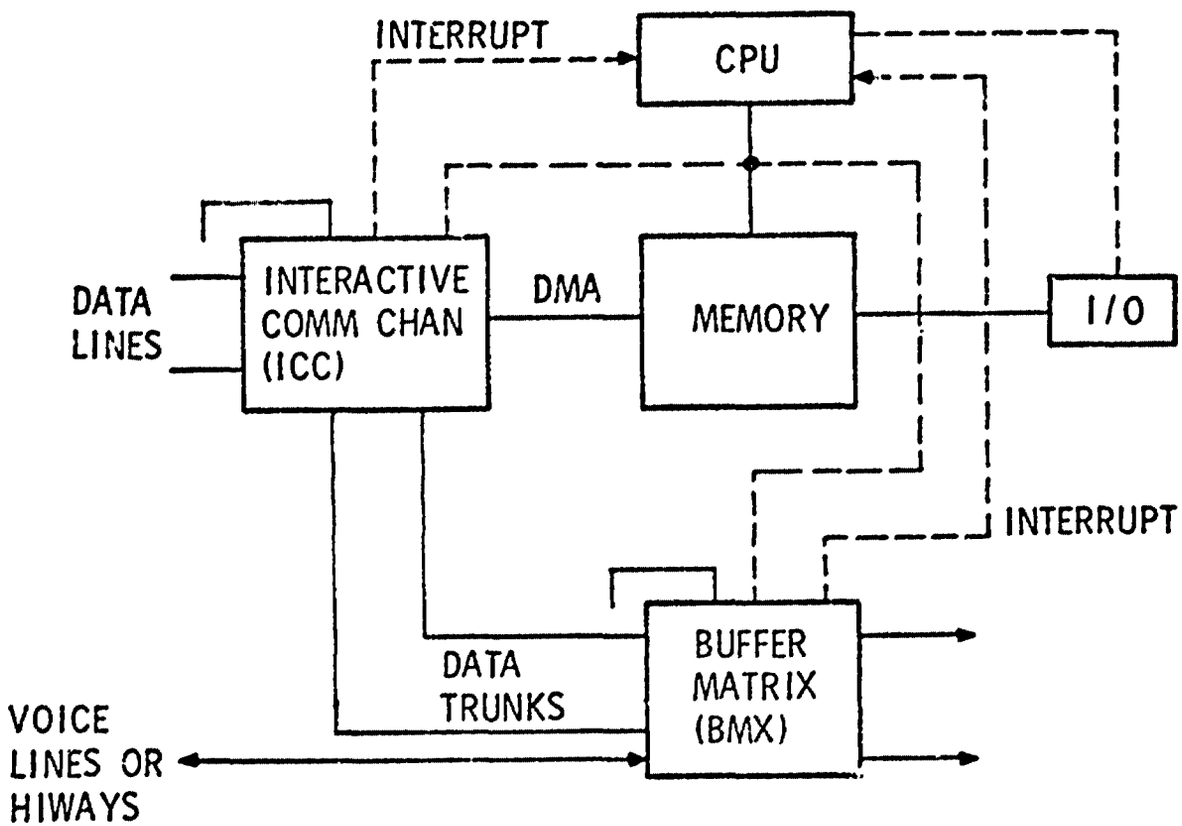


Fig. 8.4 Modified single processor

c. store/transmit data stream,

d. stuff/destuff bits, and

e. detect packet errors;

2. Software:

a. determine data buffer availability,

b. assign data buffer,

c. recognize/generate special link control messages, and

d. perform segment to header code/format conversions.

The Buffer Matrix (BMX) functions are:

1. poll subscribers (data trunks, voice lines or highways),
2. buffer voice digital bits,
3. provide small elastic buffer for data,
4. multiplex voice and data onto output trunks,
5. demultiplex voice and data on incoming trunks,
6. generate and detect sync,
7. process trunk list commands, and
8. interact with main processor for error control, buffer allocations, interrupts, etc.

Multiple processor systems (i.e. a system with a number of independent processors interconnected by buses or other means) without shared memory and with four different interprocessor communication techniques (Bus, Switch, Direct I/O Links and Transfer-Over Processor) are considered and their relative advantages and disadvantages are outlined. The disadvantages of multiple processors with shared memory are also pointed out.

A multiprocessor system is defined as follows:

1. There are two or more CPUs.
2. Main processor memory is shared and accessible by all processors.
3. I/O devices are shared by all CPUs.
4. A single integrated operating system exercises overall control of hardware and software.

All multiprocessors have common features of load sharing and throughput efficiency while contention of memory or I/O access and race conditions of handling a common function are the main problems. Various multiprocessor systems briefed in the report

include:

1. pluribus system,
2. multiport memory and central BMX,
3. multiport memory and decentralized BMX, and
4. multibus/multiport shared memory;
   a. with independent BMX, and
   b. with circuit switch.

The system performance is to be evaluated in the light of the following criteria:

1. throughput or transfer rate,
2. availability,
3. reliability,
4. expandability,
5. modularity,
6. flexibility,
7. maintainability,
8. cost, and
9. technical confidence (feasibility).

Allocating a weight of 3 to the cost, technical risk, throughput and modularity; a weight of 2 to availability, maintainability, flexibility and expandability and a weight of 1 to the reliability aspect, the performance of different systems are evaluated and the grads indicating the degree of satisfaction, are shown in Table 8.4.

The evaluation leads to the following conclusions:

1. The full configuration should contain between four to eight processors.
2. It does appear desirable to perform voice circuit switching employing a shared memory dedicated to voice which is accessed by a multiplicity of BMX controllers.
3. The multiprocessor configuration appears to offer best performance as regards throughput and flexibility.
4. The most efficient and balanced multiprocessor arrangement is a hybrid employing bussing and shared memory.
5. Multiple processor configurations can meet data node performance requirements and are in wider current usage

Table 8.4 Architecture Trade Matrix

WTS	SP	MP	MB	SM/SBMX	SN/DBMX	H/DBMX
3 Modularity	1	4	3	2	4	4
2 Expandibility	1	3	2	2	3	4
3 Risk	1	4	2	1	2	3
3 Thruput	0	2	3	0	4	4
1 Reliability	4	3	2	4	3	3
2 Availability	1	2	4	3	4	4
2 Maintainability	3	4	2	3	3	3
3 Cost	4+	4	2	4	2	3
2 Flexibility	2	2	4	3	4	4
Sum	17	28	24	25	29	32
Weighted Sum	36	59	56	46	67	75

0 To Risky
1 Poor
2 Adequate
3 Good
4 Best

SP - Single Processor
MP - Multiple Processor
MB - Bultibus
SM - Shared Memory
H - Hybrid

CBMX - Central BMX
DBMX - Decentralized BMX

then the multiprocessor arrangements. However, the multiprocessor arrangement is a better configuration from the standpoint of potential throughput performance and system flexibility. The multiprocessor approach is the recommended system provided cost differentials do not turn out to be inordinately high, in which case the multiple processor architectures are acceptable for the data network.

The recommended architecture is illustrated in Fig. 8.5. The modular distributed processor system can be expanded to have from one to eight processors. A single processor can handle at least 200 packets/second. For eight processor systems, two independent memory banks are required. It is recommended to dedicate two processors to the handling of CCIS packets. Each BMX controller has a capacity of 6.5 megabits/second and can support a maximum of 128 ports. Sixteen T1 trunks need 16 BMX controllers and thus 2048 lines can be connected to a single node.

Four independent voice shared memory banks require a throughput of 62.5 megabits/second (12.5 MBS input and 50 MBS output). Assuming halfword access (16 bit wide) the memory cycle time should not be greater than 250 nanoseconds and storage of approximately 2.5 times the sent data per frame requires 20,000 words of memory. Six ICCs have to be accommodated to satisfy the throughput requirement of nearly 12 MBS and each ICC should accommodate up to 128 access lines. Three independent 256K byte memory banks with 750 ns cycle time is needed to provide over 21 MBS throughput.

Processing of each packet requires execution of 200 to 2000 instructions. This gives the packet handling capacity of a microprocessor to be in between 100-200 and of a minicomputer between 200-600. Thus, to handle the largest traffic load (1200 packets/sec) 8 to 16 microprocessors or 4 to 8 minicomputers should be adequate. For memory addressing, a 20-bit addressing is essential. The DMA capability should also be provided. An interrupt speed of 20 microseconds or less is needed to handle 400 packets/second. Other software features include the high level language, the

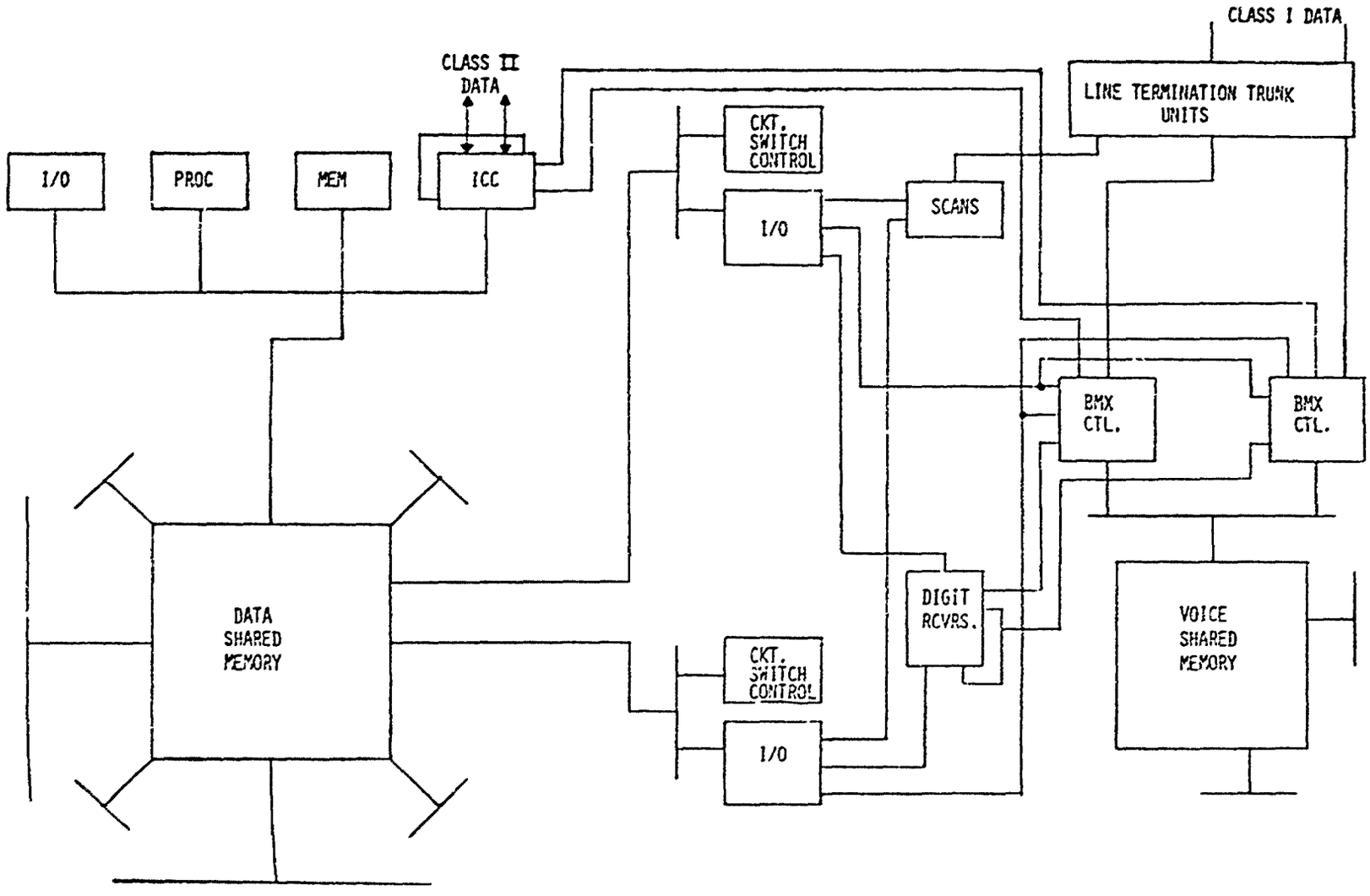


Fig. 8.5 Multibus/multiport shared memory with independent BMX.

assembler and the simulator for software tests and checkouts.

D. Node Architecture - Software

In the recommanded architecture, a single processor (with a back-up) is to be employed for control of the circuit switching function while a multiprocessor system is to be used for the packet switching function. This distinction is essential as the software has to be designed according to the hardware.

Three basic types of executive structures are currently utilized for a multi-processor configuration:

1. master-slave organization,
2. autonomous organization with multiple executive, and
3. organization with floating executive.

Their relative advantages and structural complexities are compared. When two or more processors work simultaneously on a job, the executive is expected to partition jobs for parallel processing. Also, to avoid the problem of master processor failure, a quasi-executive function must be included in the system.

The interrupt structure varies from none to one to multi-level facilities. Four ways to handle the interrupts are:

1. no interrupt capability,
2. all processor handle interrupts, and
3. program interrupt to only one processor
   a. one dedicated processor handles them, and
   b. one processor rotated around.

The use of one processor to steer the interrupts to the appropriate processor is recommended.

Another important software consideration is the processing allocation. The packet switching processing is done by putting the new item into the processor interrupt stack. The interrupt service level is called to queue the packet/segment received or transmitted for processing by the interrupt service level. This level performs actual processing and routing of new input. The normal processing level of the processor is the base level which scans all lines and initiates all non-interrupt driven processes.

The voice switching function is performed by one processor

with one back-up processor. The voice processing function is comprised of access line processing and trunk processing.

E. Interfacing the ADPT Testbed to Existing Networks

The interfacing considerations of the proposed Automatic Data Processing/Telecommunications (ADPT) with the existing ARPA and AUTODIN systems have been thoroughly investigated in the report. The important aspects having impact on ADPT/ARPA network are:

1. host-host protocol,
2. telecommunication network protocol,
3. network control program:
   a. the logging-in process,
   b. user identification;
4. ARPA net leader format,
5. interface message processor (MP) header format,
6. local/distinct/very distinct host interface,
7. special provisions for very distinct host:
   a. reliable transmission package,
   b. error detecting special host interface packet format on line;
8. host-to-IMP and IMP-to-host leader formats, and
9. ADPT simulator leader/header format.

The ADPT node includes a message switch capable of interfacing Class I and Class II terminals and can interface an AUTODIN access line. The only mechanism needed is the interchange between the message switch and the packet switch terminals. This is called a "pseudo host" and contains a software package for conversion. The main constituents of this pseudo host are:

1. pseudo-host processing input,
2. pseudo-host processing output,
3. interface to message switch, and
4. terminal routing.

The resident message switch program contains the following:

a. executive program,
b. message linkage from input line to output line,
c. line management - processing program interface,

d. input processing,

e. output processing, and

f. message exchange.

F. ADPT Testbed and Experiment Description

The ADPT testbed development includes the hardware utilization and suitable software package write-up. The hardware aspect includes an interactive communication channel, a buffer matrix and simple host devices. The software development involves the packet switch software, including ADCCP line protocol processing and source-destination segment processing and dynamic channel allocation processing. The integrated switching of voice and data traffic between unified nodes employing dynamic channel allocation has been demonstrated by a three node subnetwork simulator configuration shown in Fig. 8.6.

The processing components utilized by the ADPT testbed facility are:

1. communications processors,
2. memory:
   a. main memory,
   b. read-only memory, and
   c. scratchpad memory;
3. communications channel:
   a. bootstrap,
   b. operator's console; and
4. input/output processor.

The three node subnetwork simulator implemented by a re-entrant software program, is supported by the Time Division Multiplex Switching Matrix, the Interactive Communications Channel (ICC) and the Buffer Matrix Unit. Various functions implemented in the system are:

1. integrated switching:
   a. dynamic channel allocation,
   b. CCIS, and
   c. narrative/packet interchange;
2. circuit switch:
   a. local calls,

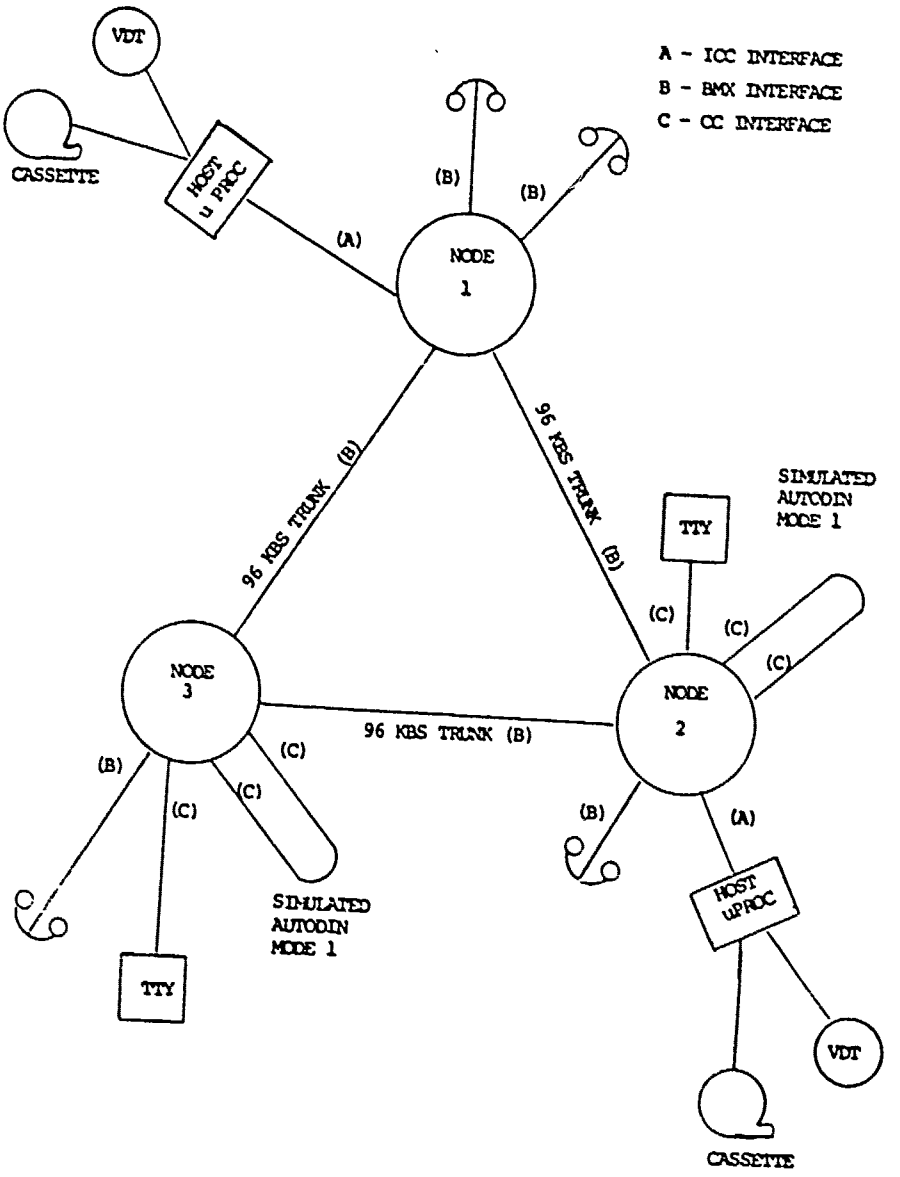


Fig. 8.6 Three node subnetwork function configuration.

b. remote calls, and

c. tandem calls;

3. message switch:

a. protocols and formats,

b. priority handling,

c. security, and

d. routing;

4. packet switch:

a. protocols and formats,

b. priority handling,

c. security, and

d. routing.

To show the functioning of unified node, three devices (CVSD Phones, silent 700 terminals and host simulator terminals) are utilized as circuit switch, message switch and/or packet switch users. The test node simulator includes the following:

1. test node simulator software package:

a. microscopic simulation, and

b. macroscopic simulation;

2. traffic generation, and

3. network simulation software:

a. simulator control unit,

b. traffic generator unit,

c. data entry/data sinks,

d. ICC simulator unit, and

e. traffic record unit.

3. Performance Characteristics

Several short experiments have been performed to demonstrate the performance of the ADPT testbed facilities. Figure 8.7 shows the node simulator configuration used. Three different input traffic tapes have been utilized in five full-length experiments. The voice traffic load is kept constant at approximately 72 Erlangs while the data intensity is varied. The test results are shown in Table 8.5. The quantitative results are presented in Table 8.6.

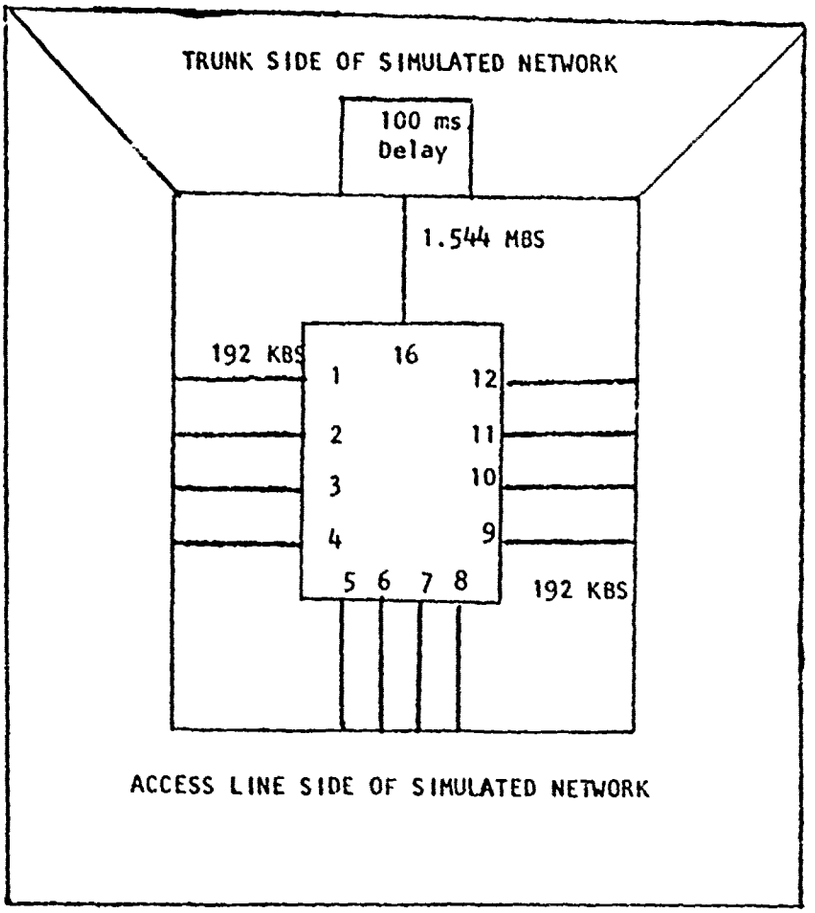


Fig. 8.7 Node simulator configuration.

Table 8,5 Node Simulator Performance Record

Run Number	Data Traffic Volume	Time Scale Factor	Run Time	Data Reduction Time
1	12,500	1	275 min.	97 min.
2A	25,000	1	330 min.	153 min.
2B	25,000	2	360 min.	170 min.
2C	25,000	4	480 min.	180 min.
3	50,000	4	600 min.	315 min.

Note - Voice traffic volume = 72 ERLANGS (16KBS per channel)

Table 8.6 Experimental Results

Run Number	Total Number of Packets	Tandem Packet Delay			Thruput		Queue Size			Trunk Utilization (%)		Buffer Utilization		Processor Utilization
			Mean	Max	Mean	Max		Mean	Max	Mean	Max	Mean	Max	
1	356,736	C	27.8	153	Input		X	1.02	7	Input		46.5	83	71.4%
		P1	32.0	195	80.9	139	C	.26	5	71.9	98.4			
		P2	32.4	230	Output		P1	.16	4	Output				
		P3	32.8	233	99.1	172	P2	.06	3	71.7	97.4			
							P3	.13	3	Voice				
										67.3	91.2			
2A	495,744	C	50.1	-	Input		X	3.15	7	Input		101.6	138	86.0%
		P1	58.0	-	112.7	149	C	.70	7	73.6	98.7			
		P2	60.2	-	Output		P1	.44	7	Output				
		P3	69.8	-	133.7	177	P2	.18	4	73.4	97.9			
							P3	.39	7	Voice				
										67.3	91.2			
2B	741,760	C	16.3	102	Input		X	1.95	7	Input		68.8	117	71.9%
		P1	20.7	151	168.4	250	C	.32	4	77.2	99.8			
		P2	21.9	296	Output		P1	.19	5	Output				
		P3	22.8	1492	206.0	301	P2	.07	4	76.5	100.00			
							P3	.16	9	Voice				
										67.3	91.2			
2C	742,272	C	5.9	97	Input		X	1.32	7	Input		63.4	118	28.0%
		P1	10.2	137	168.5	364	C	.10	3	77.2	100.0			
		P2	10.9	827	Output		P1	.06	4	Output				
		P3	10.6	1859	206.2	458	P2	.025	11	76.5	100.0			
							P3	.047	11	Voice				
										67.3	91.2			
3	1,414,270	C	9.5	83	Input		X	3.40	7	Input		103.3	185	62.7%
		P1	13.8	111	322.2	452	C	.30	3	86.1	99.9			
		P2	14.2	197	Output		P1	.16	5	Output				
		P3	14.5	529	392.9	546	P2	.07	6	84.9	100.0			
							P3	.14	4	Voice				
										67.3	91.2			

For each run, the factors indicated are the total number of packets, the mean and maximum tandem packet delay in ms for each data priorities: control (C), priorities 1-3 (P1, P2, P3), the mean and maximum queue size in number of packets for the trunk transmit queue (X) and the four associated backlog queues, the mean and maximum trunk utilization in percent, for input, output and voice, the mean and maximum buffer utilization (in percent). and the average processor utilization (in percent).

The delays encountered in the node include the transmission delay, queue delays and processing delays. Using Table 8.6, the mean available data bandwidth ($\overline{ADB}$) can be obtained as equal to 504,888 bits/sec. For a full packet containing 2048 bits, the mean transmission delay ($\overline{TD_F}$) can be obtained as approximately 2 milliseconds. The control packet containing 144 bits incurs a mean transmission delay ($\overline{TD_C}$) of 0.29 milliseconds. The maximum transmission delays TD_F and TD_C can be obtained as 15 milliseconds and 1 millisecond, respectively.

The computation of the mean and maximum queue delay for tandem control packet is given in Table 8.7. Table 8.8 shows the delay for other packets with different priorities. As no processing priorities were utilized, the processing time computed for control packets (Table 8.9) are assumed to be representations of processing times for the packets handled by the node.

4. Discussion

The RCA report describes an excellent way of designing a unified node employing the dynamic channel allocation concept. The multibus/multiport shared memory employed in the system is definitely attractive for small nodes. But for a large node, the interconnection between various modules becomes a major drawback and the memory contention problem makes it still worse. A more flexible interconnection network looks to be more appropriate. In the system, the packet switching is said to contain all necessary control and routing information. This means the originator selects the route through which the information is to be transmitted. This concept is definitely efficient for fewer nodes. But, for a network with larger number of nodes and with alternate paths, a distributed control of the route selection is more suitable. It is also not clear how much the simulated testbed can help in deciding the use of a particular routing algorithm.

Table 8.7 Computation of Queue Delays

Run. #	$\overline{X}$	$\overline{Y}$	$\overline{TD_F(ms)}$	$\overline{TD_C(ms)}$	$\overline{TW_C(ms)}$	$\hat{X}$	$\hat{Y}$	$\hat{TD}_F$(ms)	$\hat{TD}_C$(ms)	$\hat{TW}_C$(ms)
1	1.02	.26	4	.29	2.26	7	5	15	1	61
2A	3.15	.70	4	.29	6.96	7	7	15	1	63
2B	1.95	.32	4	.29	4.28	7	4	15	1	60
2C	1.32	.10	4	.29	2.86	7	3	15	1	56
3	3.40	.30	4	.29	7.38	7	3	15	1	59

$\overline{X}$: Mean number of items on the transmit queue

$\overline{Y}$: Mean number of items on the control queue

$\overline{TD_F}$: Mean transmission delay of a full packet

$\overline{TD_C}$: Mean transmission delay of a control packet

$\overline{TW_C}$: Mean time to transmit the item on the transmit and control queue and begin service of the next control packet

Λ: Indicates the maximum value of the parameter

Table 8.8 Queue Wait Time

	TW_C (ms)		TW_1 (ms)		TW_2 (ms)		TW_3 (ms)	
	Mean	Max	Mean	Max	Mean	Max	Mean	Max
1	2.26	16	2.76	92	3.16	127	3.56	130
2A	6.96	63	11.16	N/A	13.36	N/A	22.96	N/A
2B	4.28	60	4.98	98	6.18	154	7.08	1439
2C	2.86	56	3.46	96	4.16	786	3.86	1818
3	7.38	59	11.68	N/A	12.08	N/A	12.38	N/A

TW_C: Mean time to transmit the item on the transmit d control queues and begin service of the next control packet.

TW_1: Delay for priority I

TW_2: Delay for priority II

TW_3: Delay for priority III

N/A: Values not available

Table 8.9 Computation of Processing Delays

Run #	$\overline{ND}_C$(ms)	$\overline{TD}_C$(ms)	$\overline{TW}_C$(ms)	$\overline{PD}_C$(ms)	$\hat{ND}_C$(ms)	$\hat{TD}_C$(ms)	$\hat{TW}_C$(ms)	$\hat{PD}_C$(ms)
1	27.8	.29	2.26	25.3	153	1	61	91
2A	50.1	.29	6.96	42.9	-	1	63	-
2B	16.3	.29	4.28	11.7	102	1	60	41
2C	5.9	.29	2.86	2.75	97	1	56	40
3	9.5	.29	7.38	1.83	-	1	59	-

$\overline{ND}_C$: Mean delay in a node

$\overline{TD}_C$: Mean transmission delay of a control packet

$\overline{TW}_C$: Mean time to transmit the item on the transmit and control queues and begin service to the next control packet

$\overline{PD}_C$: Mean processing delay for a control packet

^: Indicates maximum value

The system is configured around two large shared memory units. It is better to have several small memory modules so that the memory contention problem can ve avoided as much as possible. The processing requirements of the system are also to be defined in more detail.

The system handles Class III traffic as Class II low priority traf- d this eliminates the delimiter needed between the two classes. ... messages are to be transmitted as highest priority Class I ...kets. The Class I calls cantain voice traffic where error checking is usually not done. It is not clear how error-checking for CCIS messages (which is very important) is to be achieved. Similarily, techniques to perform fault diagnosis and to replace the faulty units automatically have not been discussed in detail. The other area not covered in the report is the way various tables are prepared and updated at each node. The information retrieval itself is time-consuming and the associated delay should also be considered while computing the processing time of the message transmission.

CHAPTER IX

OTHER COMMUNICATION SYSTEMS

1. Introduction

The preceeding six chapters cover the potential communication processor systems recently being proposed to the Government Agencies. This section covers some of the existing important systems utilized for the communication control purpose. These also introduce the innovative ideas utilized in these systems.

2. Others Systems

Other systems briefly discussed in this chapter are:

A. Bell Labs Electronic Switching Systems,

B. North Electric ETS-4,

C. United Kingdom TXE Systems,

D. Japanese Electronic Switching Systems, and

E. French Time Division Tandem Exchanges.

A. Bell Labs Electronic Switching Systems (ESS)

No. 1, 2, 3, and 4 of the ESS family [7-10] have been developed by Bell Labs for stored-program controlled circuit switching. Each member of the ESS family was designed for its own service purposes under different technology background. With the exception of the No. 3 ESS memory units, all system units including the bus system are duplicated and a simplified system organization is shown in Fig. 9.1. When one or more functional units are out of service the effective interconnection organization must be modified appropriately.

No. 1 ESS, which has been in service since May of 1965, was designed for use in the metropolitan area where a large number of lines with heavy traffic are served. The upper and lower size limits are set at 65,000 and 4,000 lines, respectively, and the maximum capacity has been set at 1,000,000 calls in a busy hour. The

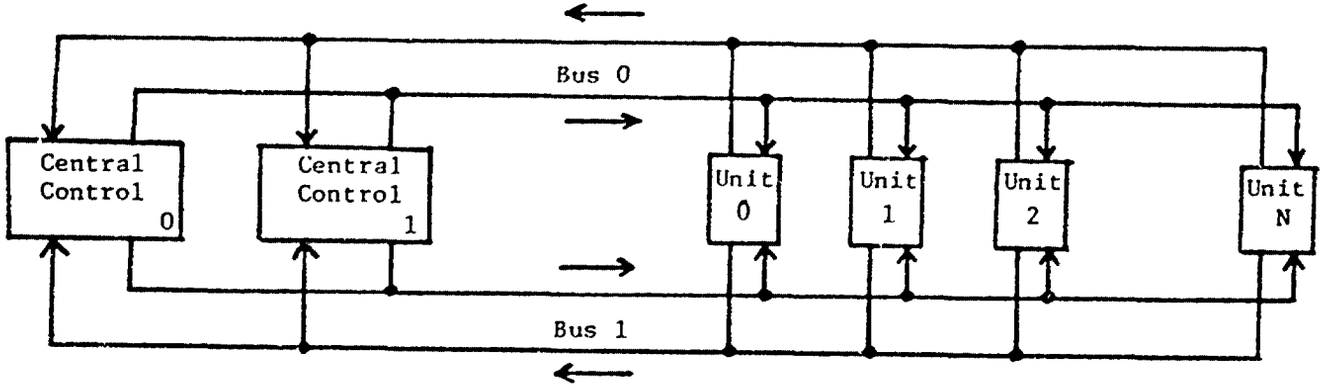


Fig. 9.1 ESS bus configuration

system consists of a switching network for making interconnections between the lines and trunks and providing access to the service circuits, a time-shared central processor consisting of a central control and the temporary and semipermanent memories for call processing, a scanner unit for monitoring the system and a distributor unit for distributing control signal. Approximately 90 totaling about 100,000 words are used to control the operations required for telephone service and to control the maintenance of the system. In brief, No. 1 ESS provides the following four functions:

1. switching network,
2. central processor,
3. scanner and distributor, and
4. stored program.

No. 2 ESS [8] was designed to complement No. 1 ESS by offering economical electronic switching service for the non-metropolitan offices of medium size ranging from 1,000 lines to about 10,000 lines. The first No. 2 ESS was placed in service on November 29, 1970. The maximum capacity was estimated to be 19,000 busy hour calls. The system uses network and other peripheral units similar to that of No. 1 ESS. The only difference of system flexibility and reliability echancement was achieved by employing two control units (only one used at a time and the second as a standby) and utilizing fewer components. Basic program and translation requirements for small No. 2 ESS offices are estimated at less than 65,000 22-bit words.

No. 3 ESS [9] was devloped in order to provide modern telephone service for the rural community. The system uses integrated-circuit techniques. The central control is implemented by using microprogram emulation. In contrast to other ESS members the call and program data are accessed through one port per central control which is associated with a single memory community. The software and hardware interlocks allowdd protection of the critical programs area. The parity checking and microprogrammed control further improved the performance. The system can handle up to

45 lines. The processing capacity is about a 2-to-1 increase compared to that of No. 2 ESS. This system has been in service since 1974.

No. 4 ESS [10] which started its service in 1976, is a high capacity versatile toll and tandem switching machine for long distance telecommunication networks. It can handle up to 107,000 trunk and service circuits and can process 350,000 long distance calls perhour. In No. 4 ESS, a time division switching network routes digital signals from incoming trunks to the proper outgoing trunks. Internal analog signals are converted to PCM digital signal by the voiceband interface unit. This system utilizes a processor which is 4 to 8 times faster, more dependable and easier to maintain than its predecessors. All units of the complex are governed by the central control unit. Other unique features included in No. 4 ESS are the processor-controlled displays, code conversions, alternate routing, centralized automatic message accounting, and standard toll mechanism. The efficient modular layout allows reduced maintenance cost.

B. North Electric ETS-4

North Electric ETS-4 [12] design is evolved from the AKE-13 that was first developed in Sweden. The ETS-4 (Electronic Toll Tandem Swtiching System, 4-Wire) is a multiprocessor controlled circuit-switching machine capable of handling up to 72,000 4-wire trunk termination . The system contains a control subsystem, a transfer subsystem, a switching subsystem, and an input/output subsystem. Fig. 9.2 shows the logical structure of ETS-4. In this system, the stored-program control function is performed by a modular multi-processor system (up to 7 control groups). Dual synchronous CPU, program and data stored units, and multiplexors implemented with high-speed IC's from a control group. The comparison of the outputs of the two processors as well as parity checking during the program execution is done to ensure the fault detection. Under the alarm condition, the supervisor initiates recovery routines

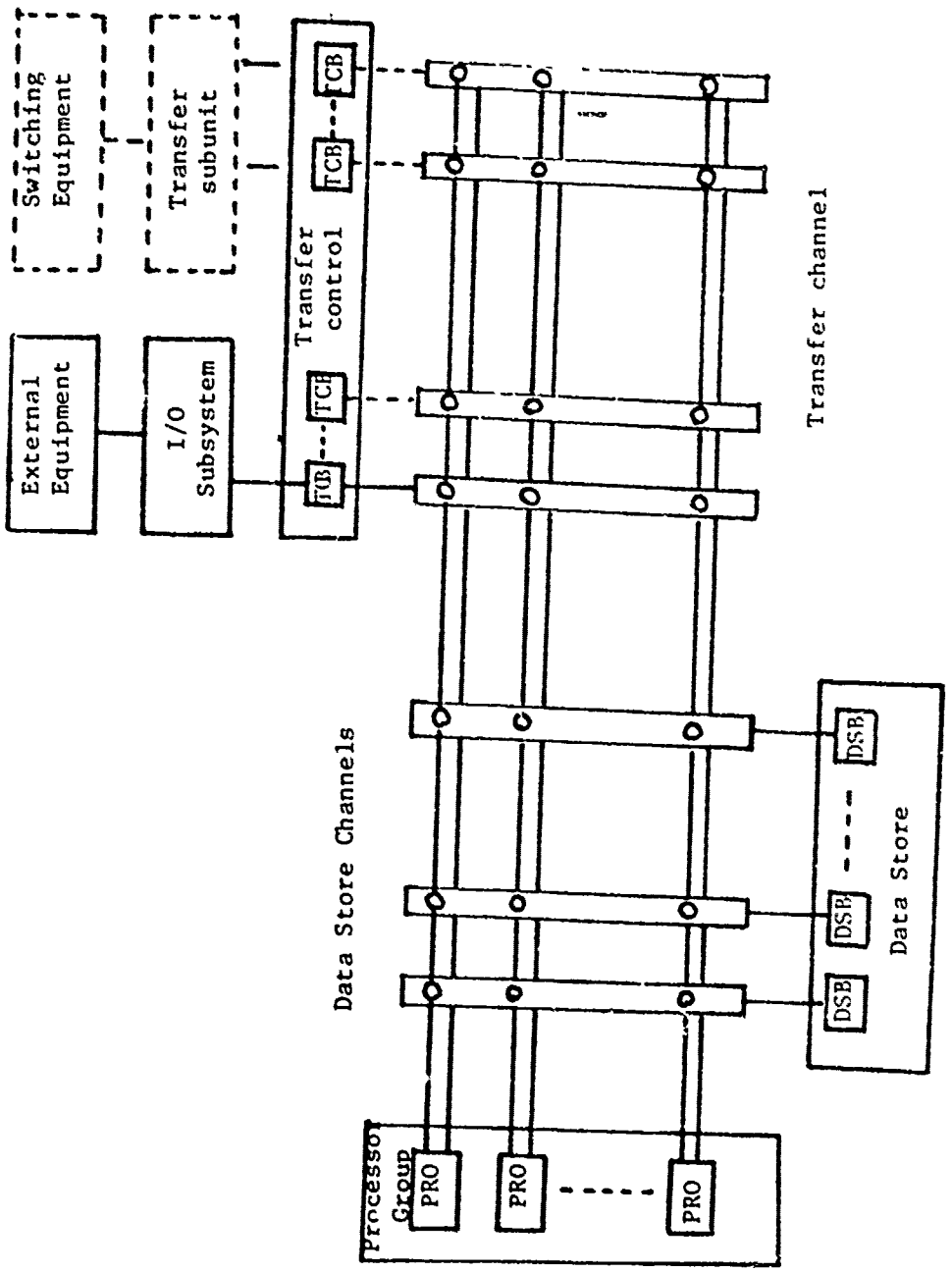


Fig. 9.2 ETS-4 basic logical structure

and supervises the reconfiguration of the system. The 4-wire communication path is provided by the switching matrix. The control of matrix code switches are managed by software consisting of approximately 3,000,000 instructions and typically 1 million words of associated data. Other software features like supervision of blocking, congestion, errors, network management, administration, test, and maintenance, etc..., are also provided.

C. United Kingdom TXE-Systems

The TXE systems have developed and used in the United Kingdom [33,34] for the telecommunication switching control function. These systems have been designed from the flexibility, considerations of service quality, maintainability, fault-tolerance, easy growth, and gradual improvement. The TXE-2 systems contains a three/four stage both way trunking network which allows the desired connections to be made between the subscribers in 50 ms. The switching elements have been implemented with discrete components. The common equipment can handle at least 7500 calls per hour and hence can cater over 2500 subscribers. An easy extension of the exchange is also possible.

The TXE-4 exchange system contains a number of divided planes of network blocks which can be accessed by the subscribers and the registers through another switching unit. The path setting functions have been achieved using simple subroutines of the control program. The result of scanning the status of each termination is constantly updated in the main control unit. Built-in check circuits and alarms have also been provided.

D. Japanese Electronic Switching Systems

The D-10, DEX-A11 and D-20 systems have been developed to fulfill the telecommunication requirements in Japan [35,36]. D-20, the latest one in the series, has been designed keeping in mind the objectives such as the range of applicability, flexibility, maintenance, and administration, miniaturization of the system, economic considerations, etc... The central processor system consists of central controls, magnetic drum channels,

magnetic drums (maximum 20 megabits), temporary memories (65 k) and a multiplex channel. The central control unit is duplicated and redundant temporary memories are provided to allow a stand-by system. The quantity of required equipments and the programs essential for the administration is reduced by associating and designing the central control unit, the magnetic drum and its channel as a single switchable entity.

The software configuration is composed of execution control, call processing, fault recovery, administration and diagnostic programs. All information on each call is concentrated in a task control block. The processor call-handling capacity is estimated as about 12,500 busy hour calls.

E. French Time Division Tandem Exchanges (E-10 System)

A time division tandem exchange of the E-10 [37] consists of several time division exchanges of 3600 path, each having its control, interconnected by PCM circuit-synchronizing groups using common channel signaling. Many ways of modules interconnections are possible. These include a single-train structure, a two-train structure and other intermediate structures. The operational characteristics of the exchange are also considered and the problems of overflow and selection time are identified. The reliability of operation depends on several factors. The organization of operations and maintenance of a tandem exchange is also given.

3. Conclusion

Several Other systems have been implemented and their detailed description is available in the literature. They have not been included in this report because of either space considerations or their limited usefulness to our current investigation.

CHAPTER X

CONCLUSION

1. Introduction

Various communication processor systems have been considered in the previous chapters. One important communication aspect is common in all the proposed CPS systems (discussed in Chapter IV through VIII) and this is the use of SENET concept (with minor modifications) for integration of voice and data traffic routing strategies have been proposed. The network simulation results as a function of important parameters have also been indicated. The most difficult job of writing this report is to compose the performance of these proposals which are the outcome of an extensive review of the existing literature and involvement of enough manpower. One of the main problems is the assumption of different functional requirements. The other limitation is imposed by the simulation process as modified network praameters and altered traffic conditions have to be assumed. In the next section, we have attempted to prepare a table comparing the parameters and characteristics of different systems. We have taken all necessary procautions to include the exact data provided in the reports. But, because of wide variations of the utilized techniques, some discrepancies are unavoidable and they should not be misinterpreted.

2. Comparison

Table 10.1 shows the comparison of various proposed systems. Time delays as a function of several parameters have veen included in individual proposals. But it is hard and unwise to come up with some relative figures. Some of the useful techniques discussed in these proposed schemes, have been utilized in arriving at our recommendations for an ideal communication processor system.

3. Concluding Remarks

Among the various proposed systems, it is rather unwise to conclude that one system is better than another. All the systems have their own unique features and certain good points as well as shortcomings. More extensive analysis and cerification is essential. The use of SENET

Table 10.1 Comparison of Communication Processor Systems

Item	North Electric CPS	GTE Sylvania SENET-DAX	Carnegie-Mellon C.mmp	Honeywell Associative Processing	RCA Unified Node
1. Transmission concept used	Circuit, message and packet	SENET integration of voice and data	SENET integration of voice and data	Integration of voice, interactive and bulk data, Class IA line switched, others packet switched	Circuit, message and packet switching
2. Frame period/ size		10 or 20 msec, 1000-2000 bits packets	10 msec, 15440 bits/ frame with 00-2200 bits packets	10 msec	10 msec, 2000 bits packets
3. Treatment of Class III traffic		Used as Class II traffic	No distinction between Class II and Class III	Separately considered	Treated as Class II lower priority data
4. CCIS messages		Subset of Class II	Sent as Class I data	Class II with highest priority	Class II data
5. Total number of lines terminated at a node	50-400 lines	100 T-1 trunk lines		16 T-1 trunk lines	
6. Total number of dedicated Class I voice lines terminated at a node	50-150 lines	3000 lines			280 lines

7. Total number of packet - switched lines at a node	5-15	372			210 lines
8. Number of indicators				32 associative memory tables with 32 words x 50 bits each	6000 bit length table
i. Route Indicator	2000				
ii. Destination entry	3000				
9. Number of lines per switch and transit storage					
i. Packet switch	40 of 20K				
ii. Store and forward switch	170 of [illegible]				
iii. Base distribution	380 Of 120K				
10. Data/Voice traffic ratio				15%	5-15%
11. Average message length	500 packets				
12. Throughput	20-95K				12 MBS/node
13. Traffic by line speed					
i. Low	0-5%	20%	20%	25%	
ii. Medium	5-85%	65%	65%	50%	

iii. High	10-15%	10%	10%	25%		
iv. Very high	85-0%	5%	5%			
14. Proposed architecture	Modularized multi-processor system with a big connection matrix	Nodal multi-processor distributed system	Multi-processor system with shared memory	Nodal associative processor systems	Multibus/ multiport shared memory system	
15. Number of processors at each node	5				8	
16. Memory module size	65K bytes	81060 bytes for tandem nodes, 28950 bytes for regional node	65K bytes	1290 FIFO buffers of sizes varying from 80 to 3000 bits each	2 memory banks for buffer matrix with capacity of 6.5 M bits each, 3 memory banks for data with capacity of 256K bytes each	
17. Memory speed	250-500 ns	1.036 microsec for regional node, 370 nsec for tandem node		500 ns for 32 bit word length	700 ns	
18. Memory-processor interconnection	Multi-stage switching matrix	Dedicated memory for each processor with bus-system for inter-processor transfer.	Cross-bar switches	Multiport memory	Multibus/ multiport system	

concept for an efficient integration of voice and data traffic and its impact on the processor architecture is very important. It is very clear that this is the only way for satisfying the future communication requirements. In the following, we have prepared our recommendations for such a system. These are only the guidelines and further detailed investigation is expected to lead to the complete structure of the system. The following identified design strategies are to be utilized:

1. Modified SENET concept with Class III treated as Class II traffic is to be utilized for the trunk calls. For local calls, circuit switching seems to be still attractive. The modularized design, multistage network implementation and distributed control show a great promise for overcoming most of the problems prevalent in the present day circuit-switching technology.
2. Frame-size is to be 10 msec. This looks to be an optimum size as a larger size frame necessitates increased time delay for the information transmission while the smaller size frame greatly affects the transmission efficiency (i.e. the ratio of the actual information content and the frame size).
3. Class III traffic should be treated as low-priority Class II data. This avoids the use of any demarkation between the two classes. This makes the control simpler and increases the information ratio.
4. CCIS is to be treated as Class II data with the highest priority. Its transmission as Class II provides the error-checking and highest priority allocation allows its inclusion in the frame as soon as it is ready to be transmitted.
5. Multi-microprocessor architecture with interconnection switches seems to be suitable to provide enough flexibility, modularity and graceful degradation in the system. It is probably better to have a larger number of multiport memory modules (with comparatively smaller capacity) rather than having a single-port, large shared memory.
6. Routing control and composition/decomposition of packets should be done using an associative memory table look-up technique. The parallelism inherent in associative memory makes the desired search pretty fast and in turn makes the process faster.

7. Preparation of a suitable and efficient software is of paramount concern and much more emphasis should be given to this area. The sky-rocketing cost of software development itself substantiates the importance of this conclusion.
8. On-line fault-diagnostic strategies should be developed and an extensive off-line testing software should be carefully prepared. System reliability has definitely improved by the LSI technology. On the other hand, an ever-increasing number of components inside a single chip augments its unreliability and necessitates its testing. More-over, a limited number of input-output leads with such a logic complexity makes the testing procedure much more complicated and a fresh approach is desirable.

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